

**RELEVANT PRODUCTS**

- ALT6701, ALT6702, ALT6704, ALT6705,  
 ALT6707, ALT6708, ALT6712, ALT6713,  
 ALT6714, ALT6720, ALT6738, ALT6740

**GENERAL DESCRIPTION**

ANADIGICS HELP4™ 3 mm x 3 mm power amplifier modules are designed for use in LTE handsets and data devices. RF inputs and outputs are internally

matched to provide optimum performance in a 50 Ω system with a minimal of external components required for proper RF bypassing.

**Table 1: Module Pin Description**

<b>PIN</b>	<b>Name</b>	<b>Description</b>
1	V <sub>BATT</sub>	Battery Voltage
2	RF <sub>IN</sub>	RF Input
3	V <sub>MODE2</sub>	Mode Control Voltage 2
4	V <sub>MODE1</sub>	Mode Control Voltage 1
5	V <sub>EN</sub>	PA Enable Voltage
6	CPL <sub>OUT</sub>	Coupler Output
7	GND	Ground
8	CPL <sub>IN</sub>	Coupler Input
9	RF <sub>OUT</sub>	RF Output
10	V <sub>CC</sub>	Supply Voltage

REFERENCE DESIGN BOARD

The board shown in Figure 1 was designed on VT47 material, 5 mils thick.

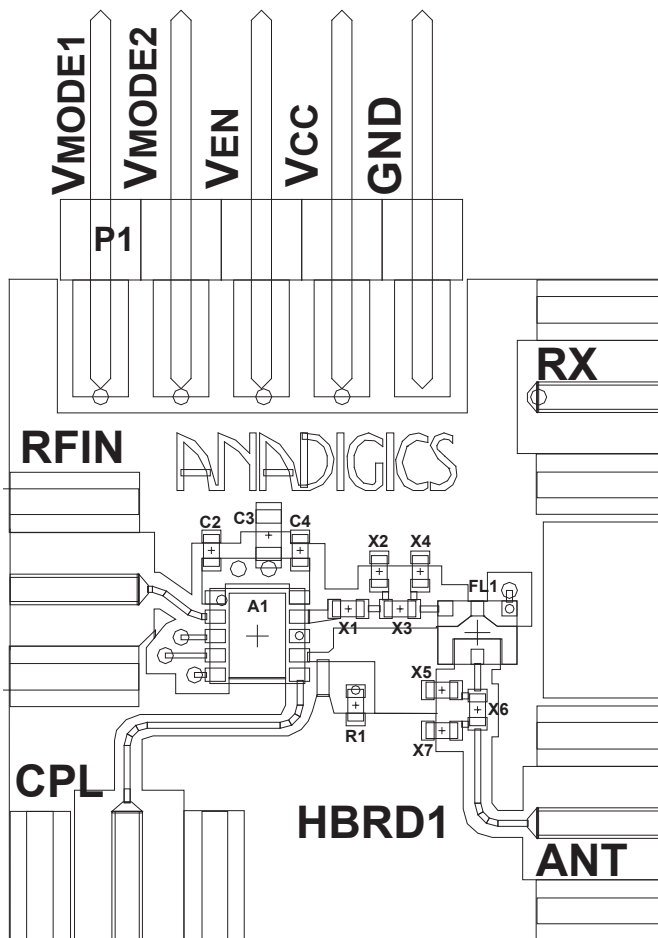
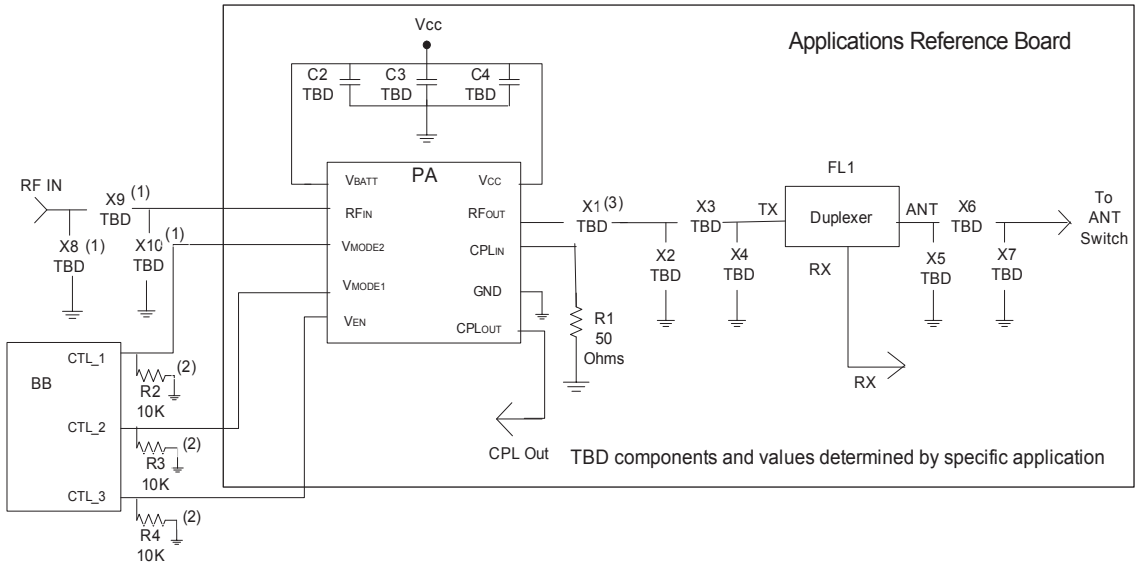


Figure 1: Applications Reference Design Board Layout



**Notes:**

- (1) Optional input matching circuit.
- (2) Optional 10k pull down resistors for control lines.
- (3) 68 pF blocking capacitor required for ALT6713.

**Figure 2: Applications Reference Design Board Schematic**

## TEST SET-UP PA FDD Analysis

### Recommended Test Equipment (Reference Fig. 3)

1. Vector Signal Generator
  - i. Optioned for digital modulation standards
2. Spectrum Analyzer
  - i. Standard measurement options preferred
  - ii. Frequency range to cover harmonics of interest.
3. Power Meter
  - i. Recommend total of 4 channels
  - ii. Sense heads should cover frequency/ power range of interest and bandwidth of modulation.
4. Power Supply
  - i. Recommend 4 channels minimum
  - ii. 1 channel should be capable of ~1A @ 5 V and have remote sense capability
  - iii. Supply lines and sense lines should be close as possible to DC power ports.  
Minimum ~16 ga. wire recommended.
5. Directional couplers with good directivity
6. ~20 dB power attenuator with good VSWR

### Equipment Presets

1. Vector Signal Generator
  - i. Select modulation
  - ii. Reduce RF power to minimum
  - iii. Turn RF output power OFF
2. Spectrum Analyzer
  - i. Assure adequate RF input attenuation to assure overload protection
3. Power Meter
  - i. Measure and set offsets for each frequency of interest.
4. Power Supply
  - i. Set Over-voltage trip for ~6 V
  - ii. Set V<sub>cc</sub> channel for over-current protection ~800 mA
  - iii. Set remaining over-current settings for ~100 mA
5. Do not apply more than +10 dBm of RF input power at any time.

### Turn-on procedure

1. Assure all RF/DC power is OFF
  - a. HOT SWITCHING IS NOT RECOMMENDED!
2. Connect DUT DC power
3. V<sub>cc</sub> connection should be on high current line and sense lines as close to device as possible.
4. Connect RF connections, torque to specification
5. Turn on DC power set for levels recommended on DUT data sheet
6. Check for quiescent current
7. Apply RF power and set for desired RF output level stepping slowly from minimum signal generator power

### Turn-off sequence:

1. Turn off RF input power
2. Turn off DC power
3. Remove DUT

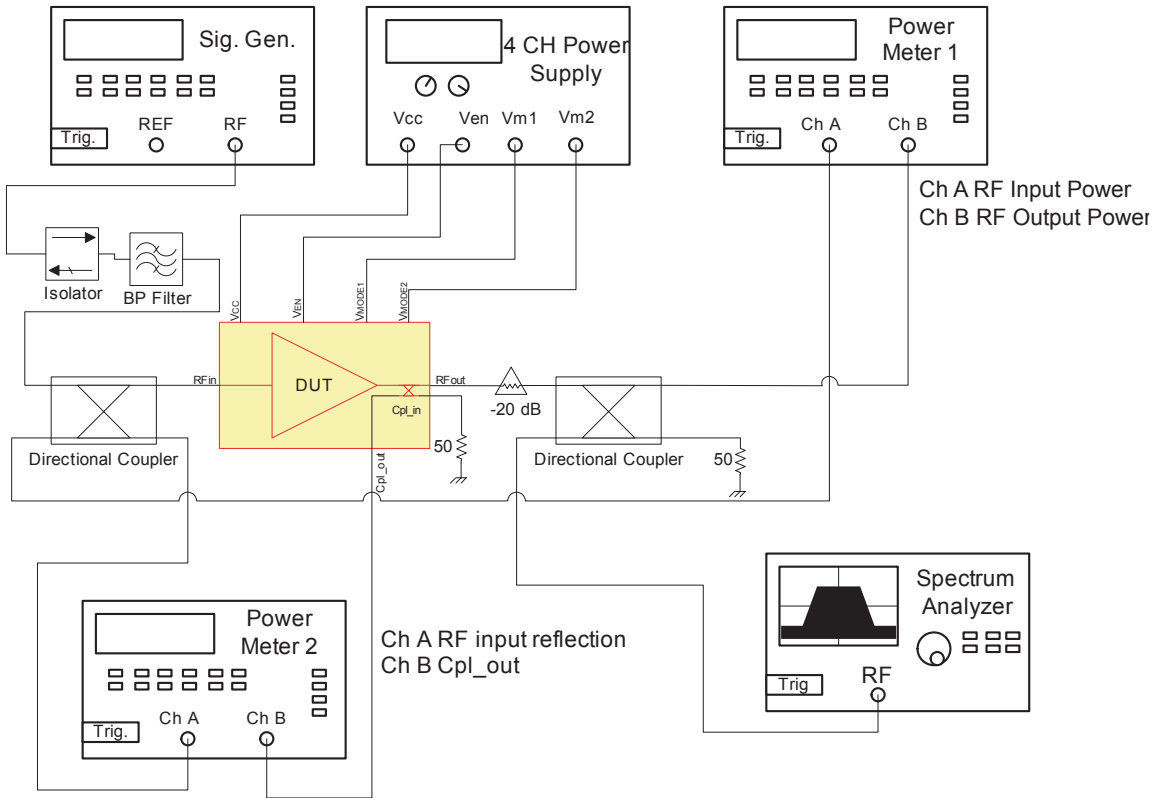


Figure 3: Test Setup Diagram 1

LTE Settings

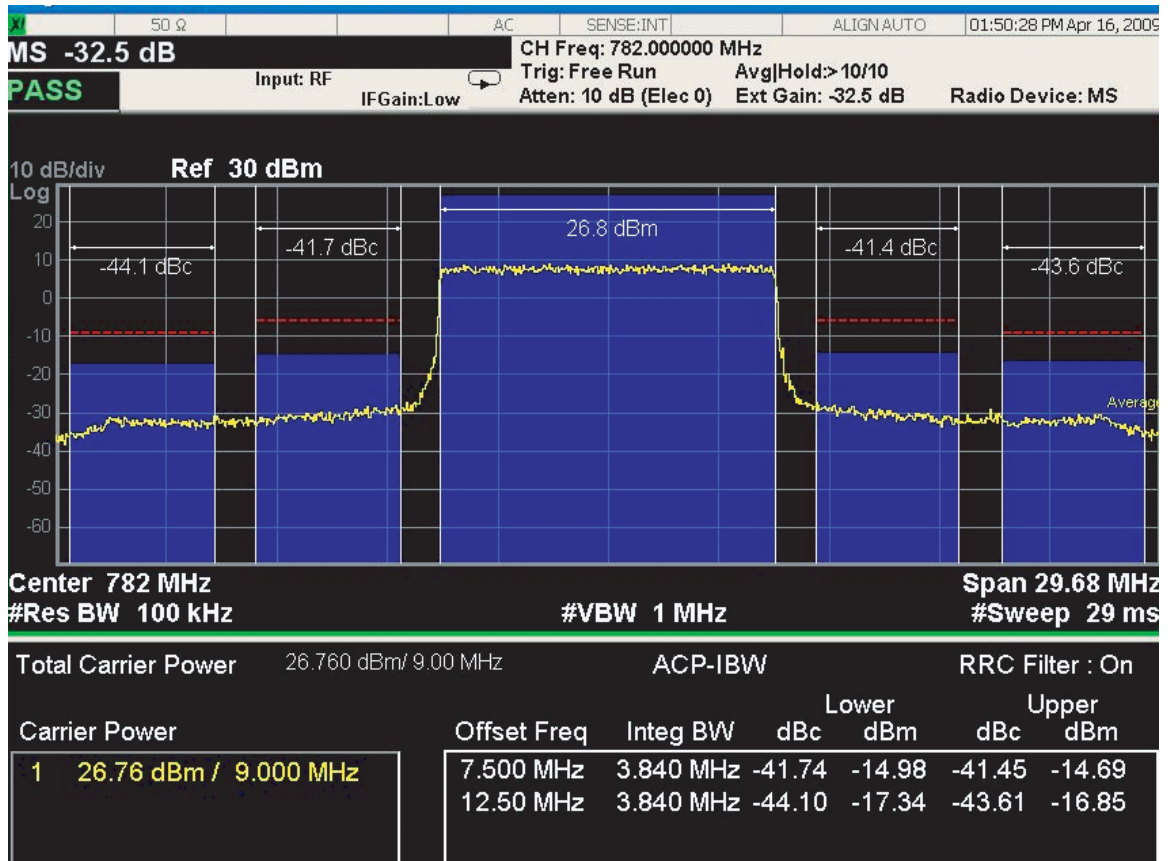


Figure 4: LTE Equipment Settings

Notes:

Spectrum Analyzer: E-UTRA to UTRA

Channel Bandwidth: 9 MHz

Offset1: 7.5 MHz

Offset2: 12.5 MHz

Offset Bandwidth: 3.84 MHz

Signal Studio Settings: PA Specification 10 MHz QPSK, 12 RB

Configuration : LTE DL 1 Carrier (2008-03)

Carrier	State	Radio Format	Configuration	Frequency Offset	Power
Carrier...	On	Basic LTE FDD Uplink (2008-03)	Full filled QPSK 10MHz (50 RB) [...]	0.000000 Hz	0.00 dB

Waveform Attributes Hint

1. Basic

Waveform Name	12RB_Q
Comment	10MHz_12RB QPSK
1/2x Sample Points	
I/Q Map	Normal

2. Marker

Marker 1 Source	Frame
Marker 2 Source	None
Marker 3 Source	RF ALC Control
Marker 4 Source	RF Blanking Control

CCDF | Waveform |

Figure 5: Signal Studio Settings 1

Configuration : LTE DL 1 Carrier (2008-03)

Carrier	State	Radio Format	Configuration	Frequency Offset	Power
Carrier ...	On	Basic LTE FDD Uplink (2008-03)	Full filled QPSK 10MHz (50 RB) [...]	0.000000 Hz	0.00 dB

Carrier 1 - Basic LTE FDD Uplink (2008-03) Hint

State: On

Channel Configuration: Full filled QPSK 10MHz (50 RB)

Waveform Generation Length: 1 frame (10ms)

Diversampling Ratio: AUTO

Pre-Filter Clipping: 100.0 %

Post-Filter Clipping: 100.0 %

1/2x Sample Points: -307200 Points

Frequency Offset: 0.000000 Hz

Power: 0.00 dB

Timing Offset: 0

Initial Phase: 0 Deg

Symbol Roll-off Length: 0 Ts

Baseband Filter: On

CCDF | Waveform |

Figure 6: Signal Studio Settings 2

Configuration : Full filled QPSK 10MHz (50 RB) (Modified)

UE Setup  Hint

1. Cell Parameters

Cell ID	0
First M-Sequence for Scrambling Code Generator	1
RNTI	0
System Bandwidth	10 MHz (50RB)
Total number of Resource Blocks	50
Total number of Occupied Sub-carriers	600
Sub-carrier Spacing	15 kHz
Cyclic Prefix	Normal
Number of Subcarriers for Resource Block	12
Number of Symbols for Resource Block	7
PUSCH DFT Swap	On
Pre-coding number for PRBS	1600

2. Sounding Reference

State	Off
Subframe Assignment	0
Power	0.00 dB
Resource Block Size	25
Resource Block Offset	0
Symbol Position	First Symbol
Group Index	0
Sequence Index	0
Cyclic Shift	0

Figure 7: Signal Studio Settings 3

Configuration : Full filled QPSK 10MHz (50 RB) (Modified)

#	Channel	State	Power	Data	Physical Channel Numbers
1	UL-SCH	On	0.00	PNS	2
2	UL-SCH	On	0.00	PNS	3-10
3	UL-SCH	On	0.00	PNS	1

Transport Channel 1 - UL-SCH  Hint

Transport Channel Number	1
Name	UL-SCH
State	On
Power	0.00 dB
Physical Channels	2
Coding State	Off
Data	PNS

Legend: ■ Cell-specific RS ■ Physical Channel ■ Transport Channel

Figure 8: Signal Studio Settings 4

Signal Studio Settings: PA Specification 10 MHz QPSK, 12 RB

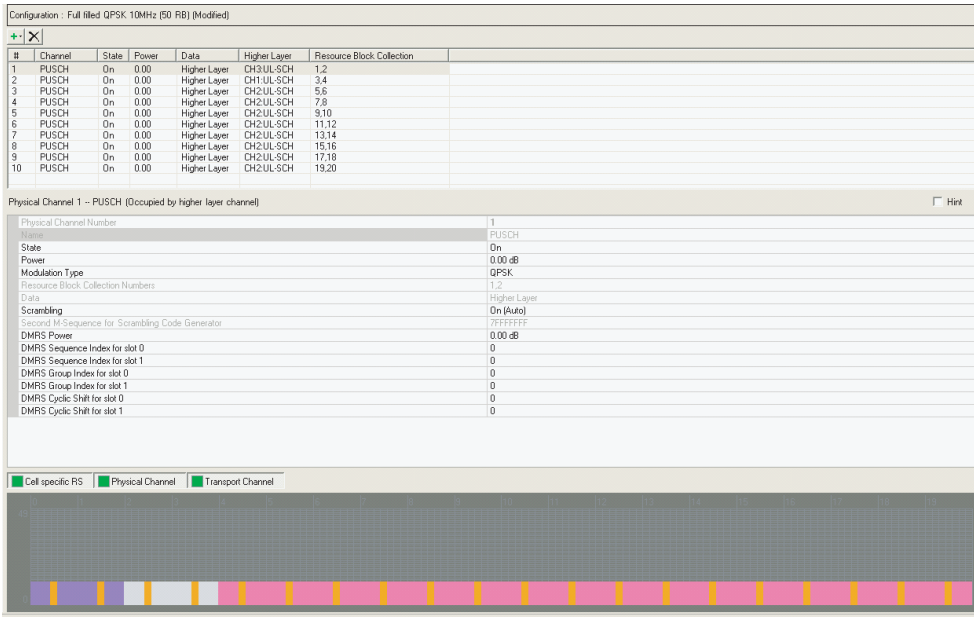


Figure 9: Signal Studio Settings 5

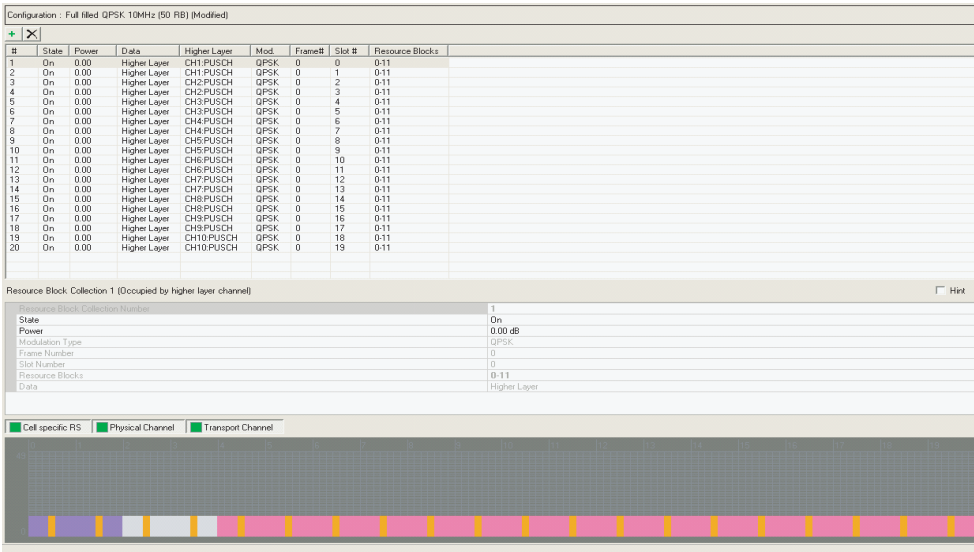


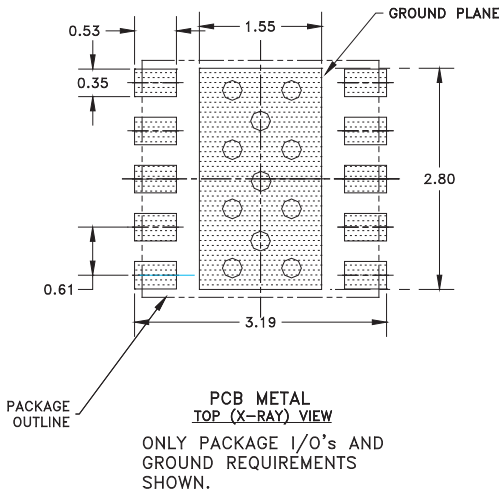
Figure 10: Signal Studio Settings 6

**PCB Board Design Guidelines**

Refer to **Figure 11** for the recommended PCB metal design, soldermask design, and stencil print patterns when assembling with ANADIGICS modules [3].

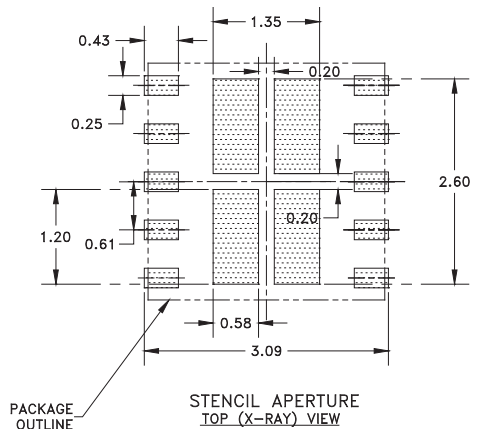
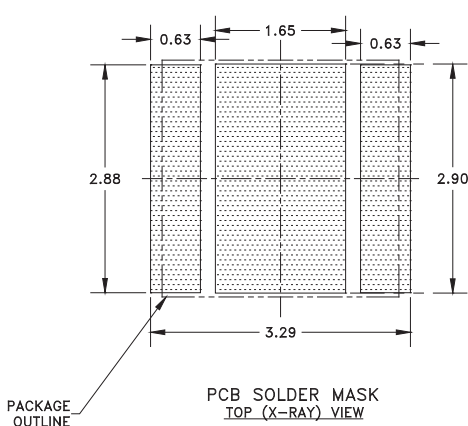
It is important to note that the PCB metal design is dependent upon several factors: the electrical and thermal performance requirement of the product and the PCB-to-device interconnect pattern.

PCB metal design recommendations primarily deal with the PCB-to-device interconnection. Specific board-level electrical and thermal performance requirements will be dictated by the physical geometry of the specific application and are the responsibility of the end product manufacturer.



NOTES:

- (1) OUTLINE DRAWING REFERENCE: P8002478\_E
- (2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.
- (4) VIAS SHOWN IN PCB METAL VIEW ARE FOR REFERENCE ONLY. NUMBER & SIZE OF THERMAL VIAS REQUIRED DEPENDENT ON HEAT DISSIPATION REQUIREMENT AND THE PCB PROCESS CAPABILITY.
- (5) RECOMMENDED STENCIL THICKNESS: APPROX. 0.150mm (6 Mils)



**Figure 11: PCB Board Design Guidelines**

## Thermal Considerations

In PA module very little heat is dissipated to the air through the top surface of the mold compound. The major thermal path for heat dissipation from the heat sources on the device is the path from the die to the package substrate to the PCB, and through the PCB surfaces to the air.

The efficiency of heat dissipation (measured by the device junction temperature) is largely dependent on the thermal resistance of the package and the PCB (including the thermal resistance of the PCB to the ambient air):

$$T_j = \Delta T_{ja} + T_a = P (R_{Pkg} + R_{PCB}) + T_a$$

where,

- $T_j$  is the junction temperature of the PA
- $T_{ja}$  is the temperature difference between the junction and the ambient
- $T_a$  is the ambient temperature
- $P$  is the total power dissipation from the PA
- $R_{Pkg}$  is the thermal resistance of the PA package
- $R_{PCB}$  is the thermal resistance of the PCB and PCB to ambient air.

For a given maximum junction temperature,  $T_j \text{ max}$ , the maximum power that can be dissipated through the package and the PCB to the ambient air is determined by:

$$P_{\text{max}} = \frac{T_j, \text{max} - T_a}{R_{Pkg} + R_{PCB}}$$

This shows that in order to reduce the junction temperature or to dissipate more power from the device, the thermal resistance of the package, the PCB, and the PCB to ambient air must be minimized. Thermal resistance of the package is determined by the package size, materials, and structures. High thermal conductivity die attach materials are used. Thermal vias and large metal pads are implemented in the substrate to minimize the thermal resistance and enhance the efficiency of the heat dissipation from the device to the PCB.

When assembled onto a PCB, the package center ground pad for an effective thermal path. Almost all the heat generated from the package must eventually dissipate through the PCB to the air.

Since the PCB-to-air thermal resistance is the major portion of the overall thermal resistance, appropriate design of the system PCB and proper assembly of the package onto the PCB are crucial to overall system thermal performance.

The following guidelines should be considered for PCB designs and board level assembly:

Optimize the board level attachment process and minimize the voids in the solder joints.

Maximize the common ground copper planes in the PCB at the top and bottom surface. More copper content in the inner layers of the PCB can also help reduce the thermal resistance of the PCB.

Ensure sufficient thermal vias connect the top and bottom ground copper planes in the PCB. These are most effective when as many as possible are placed under the PA ground pad. Effectiveness of thermal vias diminishes the farther from the package ground pad they are placed.

Minimize the interaction of the PA package with other heat sources on the PCB. Heat sources near the package can increase the PCB temperature and thus increase the ambient temperature. This is especially critical for the double-sided assembly where placement of heat sources should be avoided in the PCB area opposite to the PA. Conversely, passive components on the PCB can increase the efficiency of heat dissipation from the PCB to the air. Passive components placed near the PA package on either side of the PCB can improve the efficiency of heat dissipation from the PA package.

Increase the contact areas between the PCB and the case, such as the phone case. Heat transfer is much more efficient via conduction than convection. More contact area increases the heat dissipation to the case and eventually to the air.

In general, a larger PCB area is better for heat dissipation through the PCB to the ambient air. A large PCB should be used to allowable by the system design.

### Thermal Vias

To improve thermal and electrical performance of a mounted PA module, an array of thermal vias placed on the ground pad should be connected to the internal and bottom common ground copper planes of the PCB. The number of vias is based on via configuration and the thermal and electrical requirements of the particular module under consideration. In general, there is a direct correlation between the thermal via cross-sectional area and the heat dissipation rate. However, the heat dissipation rate through thermal vias can be easily saturated once it is greater than that of solder joint or package heat sink. Large and excessive thermal vias may introduce more voids in the solder joint and actually reduce overall heat dissipation performance.

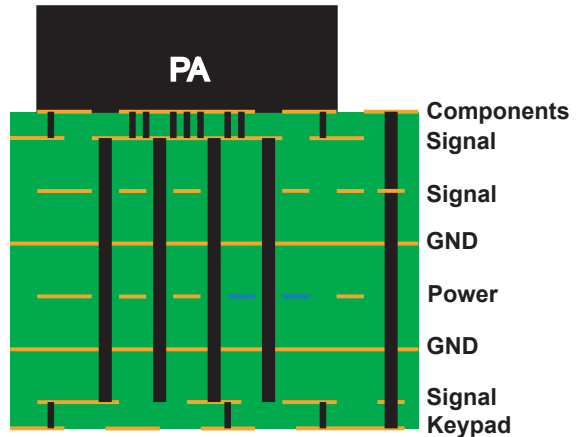
Recommended thermal vias are 0.30 mm to 0.33 mm in diameter, via barrels should be plated with 1 oz. of copper to plug the vias. The thermal via array should be arranged evenly with a pitch of 0.5 mm to 1.2 mm, depending on the form factor of the package. For the exposed region of the ground pad, if the plating thickness is not sufficient to effectively plug the barrel of the via when plated, solder, mask should be used to cap the vias with minimum dimension equal to the via diameter plug 0.1 mm. This will prevent solder wicking through the thermal via during the soldering process, resulting in voiding.

Another way to plug thermal vias uses solder mask tenting on the bottom of the copper plane. Solder mask tenting must completely cover the vias.

### GROUNDING

Good grounding is crucial for best performance. “Local ground planes” only connected to the board GND plane using a few microvias is not adequate. All GND planes must be connected to the main GND layer (one designated inner layer of the PCB) using a lot of through vias. Besides being the reference for the all RF and other signals, the GND plane is also used to distribute the heat dissipated by the PA and should therefore be sufficient size and with many through vias to spread the heat to other copper layers. In order to establish a good ground connection for the PA, it is necessary to assign an area on the first

inner layer to GND. Microvias will go from the large GND pad under the PA to the area on the inner layer and buried or through vias will go the rest of the way to the ground plane in the center for the board. See **Figure 12.**



**Figure 12:** Example of PCB Stack with Microvias on Top and Bottom Layers, Buried Vias From Layers 2 to 7, and through Vias from Layers 1 to 8.

## REFLOW SPECIFICATIONS

The reflow profile is a critical part of the PCB assembly process. A proper reflow profile must provide adequate time for flux volatilization, proper peak temperature, time above liquidous, ramp up and cool down rates. The profile used has a direct bearing on manufacturing yield solder joint integrity, and the reliability of the assembly [2,3]. A typical reflow profile is made up of four distinct zones: the preheat zone, the soak zone/flux activation zone, the reflow zone, and the cooling zone.

### Preheat Zone

Typically the heating rate in the preheat zone should be 2 °C to 4 °C/second and the peak temperature in the zone should be 100 °C to 125 °C. If the temperature ramp is too fast, the solder paste may splatter and cause solder balls. Also, to avoid thermal shock to sensitive components such as ceramic chip resistors, the maximum heating rate should be controlled.

### Soak Zone

The soak zone is intended to allow the board and components to reach a uniform temperature, minimizing thermal gradients. The soak zone also acts to activate the flux within the solder paste. The ramp rate in this zone is very low and the temperature is raised near the melting point of solder. The consequences of being at too high a temperature in the soak zone are solder balls due to insufficient fluxing (when the ramp is too fast) and solder splatter due to excessive oxidation of paste (when the ramp rate is too slow).

### Reflow Zone

In this zone the temperature is kept above the melting point of the solder for 30 to 60 seconds. The peak temperature in this zone should be high enough for adequate flux action and to obtain good wetting.

The temperature, however, should not be so high as to cause component damage, board damage, discoloration or charring of the board. Extended duration above the solder melting point will damage temperature sensitive components and potentially create excessive intermetallic growth between the solder and the I/O pad metallization which makes the solder joint brittle and reduces solder joint fatigue

resistance. Additionally high temperature can promote oxide growth, depending upon the furnace atmosphere which can degrade solder wetting.

### Cooling Zone

The cooling rate of the solder joint after reflow is also important. For a given solder system, the cooling rate is directly associated with the resulting microstructure which in turn, affects the mechanical behavior of solder joints. The faster the cooling rate, the smaller the grain size of the solder will be, and hence the higher the fatigue resistance of the solder joint. Conversely, rapid cooling will result in residual stresses between TCE mismatched components. Therefore, the cooling rate needs to be optimized. The profile of choice can affect any of the following areas to a different degree by one of more of the profile zones [2].

- Temperature distribution across the assembly
- Plastic IC package cracking
- Solder balling
- Solder beading
- Wetting ability
- Residue cleanliness
- Residue appearance and characteristics
- Solder joint voids
- Metallurgical reactions between solder and substrate surface
- Board flatness
- Microstructure of solder joints
- Residual stress level of the assembly

**REFLOW PROFILES**

**Table 2** provides a breakdown of the reflow conditions provided by the JEDEC standard J-STD-020C [5] for leadfree solders. While this standard specifies a peak reflow temperature of 260 °C, the actual peak temperature subjected to the part during reflow must not exceed 260 ± 5 °C.

**Table 2: Lead-free MSL Reflow Profile Breakdown**

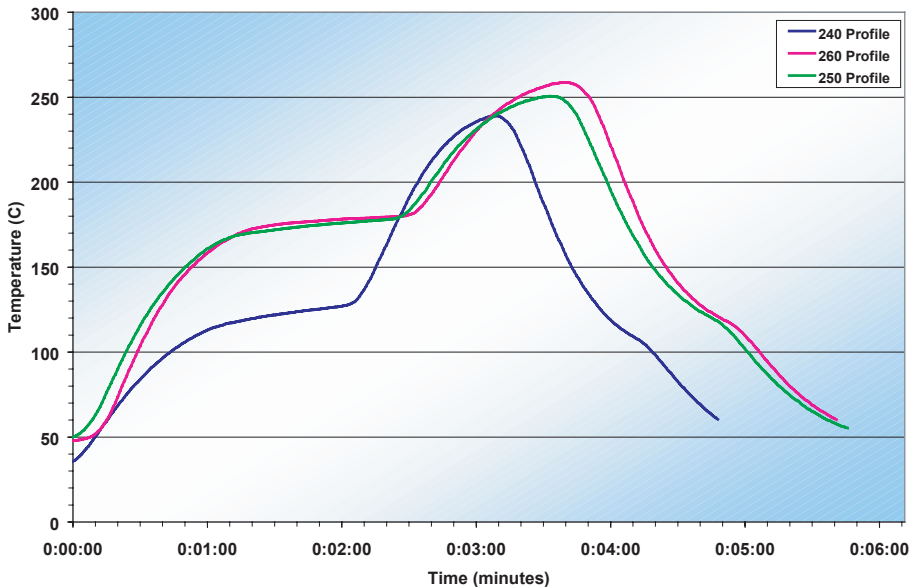
	<b>JEDEC specifications</b>
Avg. Ramp-up ( $T_L$ to $T_p$ ) <sup>(1), (2)</sup>	3 °C/second max
Dwell Time (175 ± 25 °C)	60-120 seconds
Ramp-up 200 °C to 217 °C	3 °C/second max
Time Above 217 °C	60-150 seconds
Time Within 5 °C of Peak	20-40 seconds max
Peak Temperature <sup>(3)</sup>	260 -5/+0 °C
Average Ramp-down	6 °C/second max

Notes:

(1)  $T_L$  is the solder eutectic temperature

(2)  $T_p$  is the peak temperature

(3) Actual peak temperature will be product dependent



**Figure 13: Comparison of High Temperature Reflow Profiles**

**REWORK GUIDELINE**

The most common method of repairing surface mount devices is by using hot air devices. During this rework process care should be taken to prevent thermal damage to adjacent component or substrates. The following guidelines should be used to prevent thermal damage and to produce an acceptable solder joint after repair/rework [1]:

- Characterize the rework process carefully so as not to overheat and damage the device.
- Keep the number of times a part is removed and replaced to a maximum of two.
- Preheat the substrate for about 30 minutes to about 95 °C.
- Use an appropriate attachment to direct the flow of hot air to the component to be removed or replaced.
- Minimize the heat time to reduce the device exposure to high temperatures.

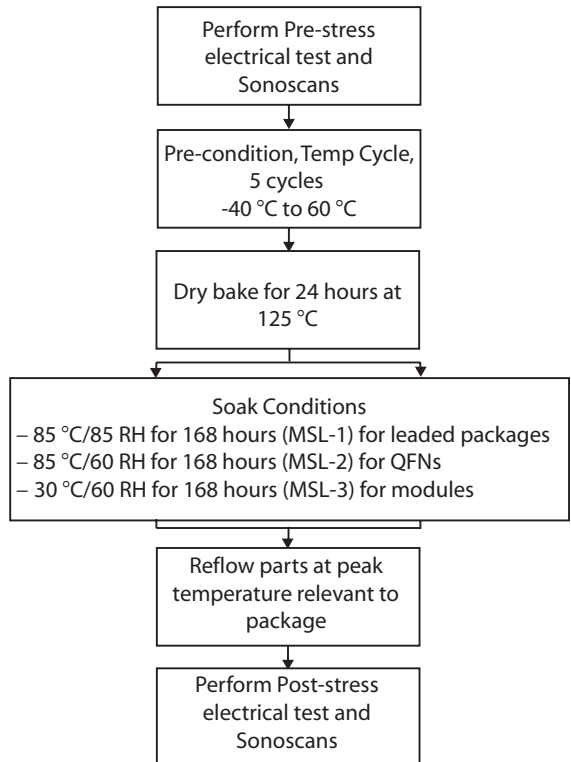
**MSL (Moisture Sensitive Levels)**

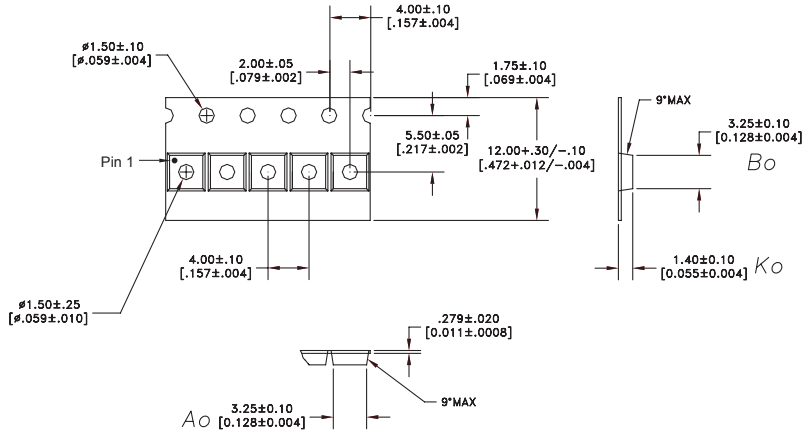
MSL levels are used to classify the sensitivity of a microelectronic package to moisture. Packages can be classified from level 1 (hermetic package) to level 6 (very sensitive). Knowledge of the MSL level of a package is crucial during 2nd level solder reflow for proper assembly of the product as these levels dictate the duration that the package can be exposed to the atmosphere before being exposed to solder reflow temperatures. Once this time limit expires, the package is at risk for catastrophic damage during reflow. **Table 3** summarizes the different MSL levels as defined by JEDEC Standards J--STD-020B and J-STD-020C [2,4].

**Table 3: Moisture Sensitive Levels**

Level	Floor Life
1	Unlimited
2	1 year
2a	4 weeks
3	168 hours (ANADIGICS product)
4	72 hours
5	48 hours
5a	24 hours
6	Time on Label

The following flowchart shows the flow of the tests performed to determine the MSL Rating:





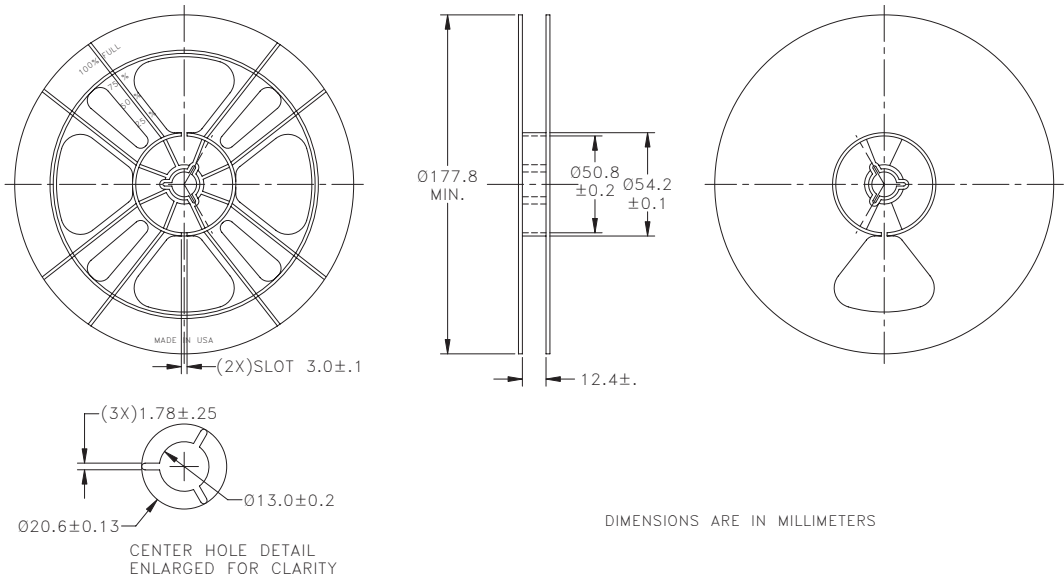
NOTES:

- 1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)  
100% RECYCLABLE.

DIMENSIONS ARE IN MILLIMETERS [INCHES]

*DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994*

Figure 14: Carrier Tape Drawing



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- 1. MATERIAL: BLACK CARBON POLYSTYRENE
- SURFACE RESISTIVITY: 1X10<sup>4</sup> TO 1X10<sup>5</sup> ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

Figure 15: Reel Drawing

## ESD (Electro Static Discharge)

ESD or Electro Static Discharge is the leading cause of electronic component failure during and after the manufacturing process. High frequency and highly miniaturized active components are especially prone to damage by ESD. GaAs MMICs are not immune, and deserve every possible ESD precaution.

ESD can damage all electronic parts, components and subassemblies at all manufacturing and handling stages. It affects production yields, manufacturing costs, product quality, reliability, and profitability. And while only a few components will be catastrophically damaged to an extent where they fail completely, many more may suffer damage that is not immediately apparent. These latent failures will cause premature failure in the field, with huge associated costs.

Thus, ESD impacts productivity and product reliability in all aspects of the electronic environment. In view of all this, the importance of effective ESD prevention cannot be overemphasized.

### GENERAL ESD PRECAUTIONS

General ESD precautions center on measures that can be taken to minimize electrostatic charge building up. Reducing static generating processes throughout the manufacturing flow should be the goal. Contact and separation of dissimilar materials and common plastics should be avoided as much as possible in the work environment. In addition, general measures to dissipate and neutralize charges should be instituted.

These include:

1. **Humidity Control.** Charge accumulation is minimized if environmental humidity levels are kept high. Forty percent relative humidity is recommended.

For instance, picking up a poly bag from a bench can generate up to 20,000 Volts of charge at less than 25% Relative Humidity, but will generate less than 1,200 Volts if the Relative Humidity is kept between 65% and 90%.

2. **Ionizers.** In situations where we have to deal with isolated conductors that cannot be grounded, and with most common plastics, air ionization can

neutralize the static charge. Because only air is required for ionization to be effective, air ionizers can and should be used wherever it is not possible to ground everything. Ionizers should also be used as a backup where grounding and other methods are also employed.

3. **Wrist straps.** Since the main cause of static is people, the importance of wrist-straps in the fight against ESD cannot be over-emphasized. A wrist-strap, when properly grounded, keeps a person wearing it near ground potential and static charges do not accumulate. Wrist-straps should be worn by all personnel in all ESD Protected Areas, that is, where ESD susceptible devices and end products containing them are assembled, manufactured, handled and packaged.

Further ESD protection, similar to wrist-straps, involves the use of ESD protective floors in conjunction with ESD control footwear or foot-straps. Static control garments (smocks) give additional protection especially in clean room environments.

4. **Work Areas.** All areas where components that are not in ESD protective packaging are handled should be designated as ESD Protective Areas. Access to such areas should be controlled, and only entered if protective measures, such as wrist-straps and ESD footwear are employed by all personnel. Workstations in such areas should have a static-dissipative work surface with a common ground for it and the worker's wrist-strap.

## HELP4™ LTE Power Amplifier Module

### REFERENCES

[1] Ray P. Prasad; Surface Mount Technology - Principles and Practice; Van Nostrand Reinhold - New York; 1989; Pages 311 -328.

[2] Charles Harper; Electronic Packaging and Interconnect Handbook; "Solder Technologies for Electronic Packaging Assembly"; McGraw-Hill 2000; Pages 6.1 -6.83

[3] <http://www.ecd.com/emfg/instruments/tech1.asp>

[4] JDEC Standard J-STD-020C. *Mositure/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices.* July 2004.

[5] ANADIGICS Application Note: Soldering Guidelines for Module PCB Mounting Revision 12.



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