Although the ACA0861D Line Amplifier IC is designed for optimum operation with a +12 VDC supply, it is possible to operate the part at reduced supply voltages, with some performance reduction.

For such an operation, a slight change in external bias conditions has to be implemented, depending on the voltage level chosen.

### Table 1: Summary of Typical Single Part Performance (1)

<table>
<thead>
<tr>
<th>SUPPLY VOLTAGE</th>
<th>+12</th>
<th>+8</th>
<th>+5</th>
<th>V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Current</td>
<td>470</td>
<td>420</td>
<td>230</td>
<td>mA</td>
</tr>
<tr>
<td>Gain</td>
<td>12</td>
<td>11.5</td>
<td>11</td>
<td>dB</td>
</tr>
<tr>
<td>CTB</td>
<td>-71</td>
<td>-68</td>
<td>-62</td>
<td>dBC</td>
</tr>
<tr>
<td>128 ch flat +36 dBmV</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>dBC</td>
</tr>
<tr>
<td>128 ch flat +32 dBmV</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>dBC</td>
</tr>
<tr>
<td>CSO</td>
<td>-73</td>
<td>-70</td>
<td>-62</td>
<td>dBC</td>
</tr>
<tr>
<td>128 ch flat +36 dBmV</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>dBC</td>
</tr>
<tr>
<td>128 ch flat +32 dBmV</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>dBC</td>
</tr>
<tr>
<td>Xmod</td>
<td>-67</td>
<td>-65</td>
<td>-57</td>
<td>dBC</td>
</tr>
<tr>
<td>128 ch flat +36 dBmV</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>dBC</td>
</tr>
<tr>
<td>128 ch flat +32 dBmV</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>dBC</td>
</tr>
</tbody>
</table>

(1) Two devices can be cascaded together for higher gain applications. See ACA0861 Data Sheet for details.

### Table 2: Connections for Proper Bias

<table>
<thead>
<tr>
<th>SUPPLY VOLTAGE</th>
<th>(Normal Operation) 12 VOLTS</th>
<th>8 VOLTS</th>
<th>5 VOLTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 2</td>
<td>No Connection (Open)</td>
<td>3.9 kΩ to GND</td>
<td>2 kΩ to V&lt;sub&gt;DD&lt;/sub&gt; (+5 V)</td>
</tr>
<tr>
<td>Pin 7</td>
<td>No Connection (Open)</td>
<td>5.1 kΩ to V&lt;sub&gt;DD&lt;/sub&gt; (+8 V)</td>
<td>1.5 kΩ to GND</td>
</tr>
</tbody>
</table>
Using the ACA0861D at +8 V and +5 V Supply Voltages

Figure 1: Test Circuit for +8 Volt \( V_{DD} \)

Figure 2: CTB at +8 V, 420 mA
128 Channels Flat, +36 dBmV Output

\[
\begin{align*}
\text{CTB (dBc)} & \quad \text{Frequency (MHz)} \\
\hline
\text{-85} & \quad 0 \\
\text{-80} & \quad 100 \\
\text{-75} & \quad 200 \\
\text{-70} & \quad 300 \\
\text{-65} & \quad 400 \\
\text{-60} & \quad 500 \\
\text{-55} & \quad 600 \\
\text{-50} & \quad 700 \\
\end{align*}
\]
Using the ACA0861D at +8 V and +5 V Supply Voltages

Figure 3: CSO at +8 V, 420 mA
128 Channels Flat, +36 dBmV Output

Figure 4: Xmod +8 V, 420 mA
128 Channels Flat, +36 dBmV Output
Using the ACA0861D at +8 V and +5 V Supply Voltages

Figure 5: S11 at +8 V

Figure 6: S21 at +8 V
Using the ACA0861D at +8 V and +5 V Supply Voltages

Figure 7: S12 at +8 V

Figure 8: S22 at +8 V
Using the ACA0861D at +8 V and +5 V Supply Voltages

Figure 9: Test Circuit for +5 Volt V_{DD}

ACA0861D

Figure 10: CTB at +5 V, 230 mA
128 Channels Flat, +32 dBmV Output
Using the ACA0861D at +8 V and +5 V Supply Voltages

**Figure 11:** CSO at +5 V, 230 mA
128 Channels Flat, +32 dBmV Output

**Figure 12:** Xmod at +5 V, 230 mA
128 Channels Flat, +32 dBmV Output
Using the ACA0861D at +8 V and +5 V Supply Voltages

**Figure 13: S11 at +5 V**

- Frequency (MHz)
- S11 Mag (dB)

**Figure 14: S21 at +5 V**

- Frequency (MHz)
- S21 Mag (dB)
Using the ACA0861D at +8 V and +5 V Supply Voltages

Figure 15: S12 at +5 V

Figure 16: S22 at +5 V
Using the ACA0861D at +8 V and +5 V Supply Voltages

NOTES
Using the ACA0861D at +8 V and +5 V Supply Voltages