

**RELEVANT PRODUCTS**

- ACA0861C

**INTRODUCTION**

Introduction

This Application Note describes the performance that is obtained when the ACA0861C 75  $\Omega$  Differential Amplifier IC is adapted for operation in a 50  $\Omega$  Single-ended mode.

**Background**

The ACA0861C is traditionally used as a “50 MHz to 1000 MHz” linear power amplifier in 75  $\Omega$  CATV distribution trunks. Components in this type of service must, by default, possess superior broadband linearity performance and be ruggedized to withstand harsh environments. These attributes make the ACA0861C especially suitable for use as a 50  $\Omega$  Amplifier in systems that depend upon highly linear and reliable components.

**50  $\Omega$  Matching Circuits**

Although the ACA0861 is optimized for broadband 75  $\Omega$  systems, it can be adapted to operate in 50  $\Omega$  systems by incorporating matching elements tailored for specific frequency segments. Any segment within the range of 50 MHz to 1100 MHz may be chosen.

Three matching circuits and the associated performance data are presented below for specific segments centered at 150 MHz, 450 MHz, and 950 MHz. Other frequencies may be utilized by modifying the values of the passive matching elements.

**Internal Block Diagram**

The internal block diagram of the ACA0861C is illustrated below in Figure 1. The IC is fabricated entirely in Gallium Arsenide (GaAs) and consists of a cascaded pair of differential amplifiers with a pair of biasing drivers.

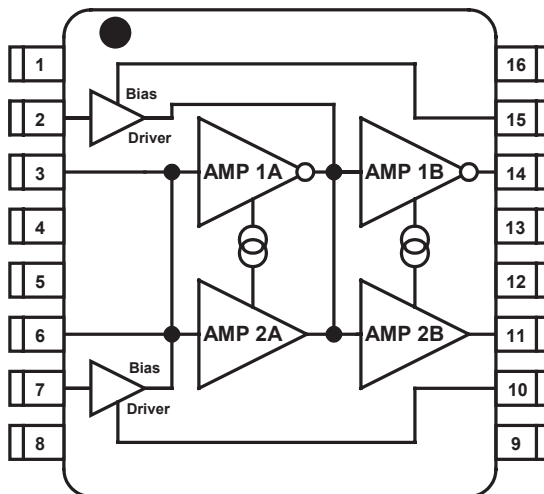
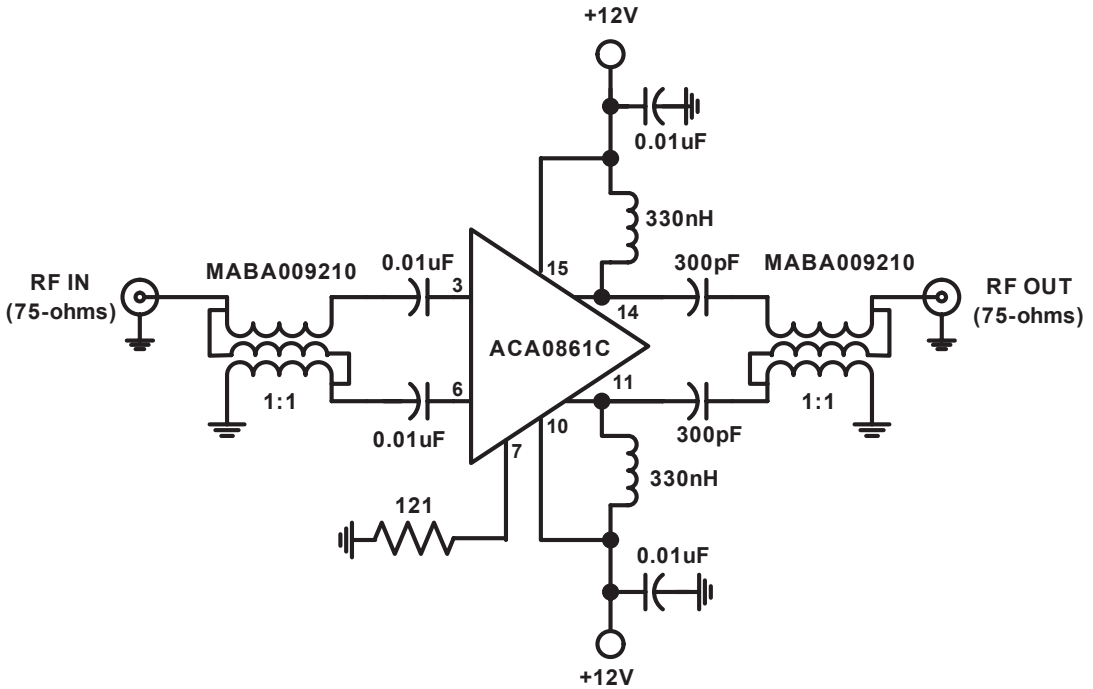


Figure 1: ACA0861 Internal Block Diagram

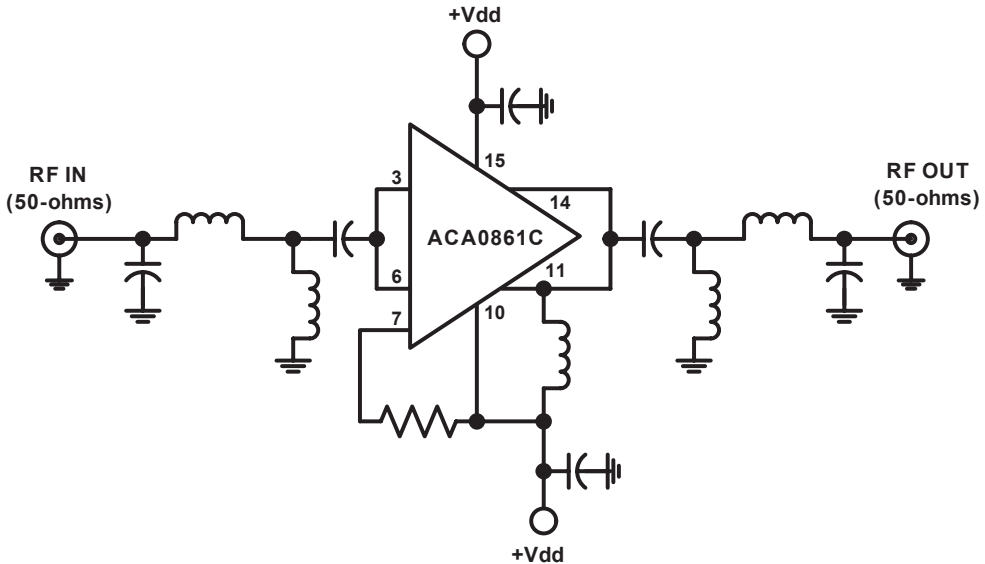
# ADAPTING THE ACA0861C FOR 50 Ω OPERATION



**Figure 2: Single-Stage Amp (#2) Configuration**

The Test Circuit pictured above depicts the amplifier in a 75 Ω, differential mode of operation. A pair of 1:1 balun transformers matches the 37.5 Ω (differential) at the input and the output ports to the system impedance of 75 Ω (single-ended). The DC supply

voltage of +12 Vdc is applied through the pair of 330 nH inductors. The biasing is set externally via a resistor placed between pin #7 and ground. The typical current consumption is approximately 260 mA.



**Figure 3: Modified Configuration (simplified)**

## ADAPTING THE ACA0861C FOR 50 Ω OPERATION

Only a few modifications to the standard 75-ohm (differential) Test Circuit are required to re-configure the ACA0861C for 50-ohm (single-ended) operation.

The baluns are removed and the two differential ports are combined into a single-ended port at both

the input and the output. High-pass and low-pass matching networks are utilized to optimize the return-loss at the desired frequency range of operation. An external bias voltage, applied to pin #7 via the pull-up resistor connected to pin #10, sets the desired I<sub>DD</sub> operating point.

## PERFORMANCE DATA - 150 MHz

Table 1: 150 MHz 12 V

| PARAMETER         | MIN | TYP   | MAX | UNITS           |
|-------------------|-----|-------|-----|-----------------|
| Frequency         | 100 | 150   | 200 | MHz             |
| V <sub>DD</sub>   | -   | 12    | -   | V <sub>DC</sub> |
| I <sub>DD</sub>   | 400 | 500   | 600 | mA              |
| Gain              | -   | 10.5  | -   | dB              |
| Noise Figure      | -   | 3.0   | -   | dB              |
| Output Power      | -   | +20   | -   | dBm             |
| OIP3 <sup>1</sup> | -   | +57   | -   | dBm             |
| P1dB              | -   | +31.5 | -   | dBm             |

**NOTE:**

1. Measured using two CW tones at an output power level of +20 dBm per tone.

Table 2: 150 MHz 8 V

| PARAMETER         | MIN | TYP   | MAX | UNITS           |
|-------------------|-----|-------|-----|-----------------|
| Frequency         | 100 | 150   | 200 | MHz             |
| V <sub>DD</sub>   | -   | 8     | -   | V <sub>DC</sub> |
| I <sub>DD</sub>   | 400 | 450   | 600 | mA              |
| Gain              | -   | 10.5  | -   | dB              |
| Noise Figure      | -   | 3.0   | -   | dB              |
| Output Power      | -   | +16   | -   | dBm             |
| OIP3 <sup>1</sup> | -   | +52   | -   | dBm             |
| P1dB              | -   | +28.5 | -   | dBm             |

**NOTE:**

1. Measured using two CW tones at an output power level of +16 dBm per tone.

# ADAPTING THE ACA0861C FOR 50 Ω OPERATION

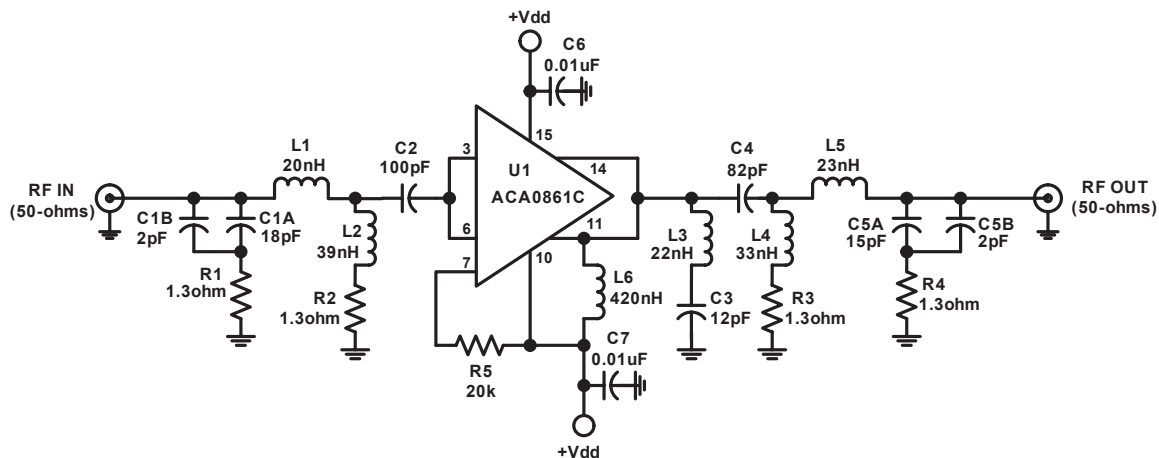


Figure 4: 150 MHz Circuit

Figure 5: 150 MHz S21 Graph

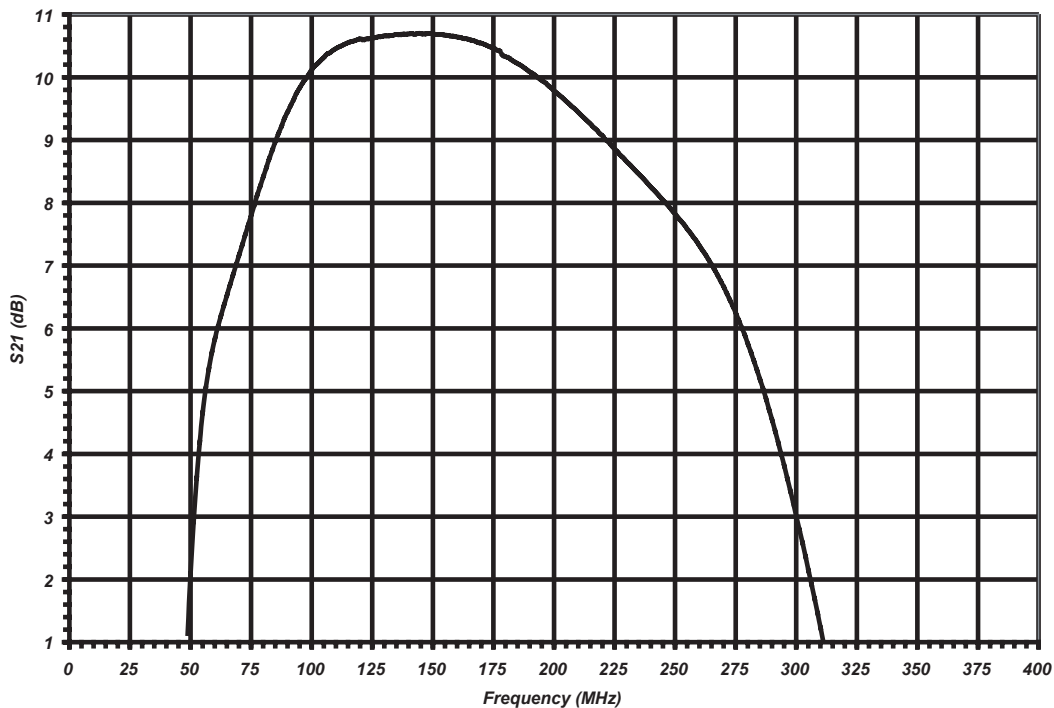


Figure 6: 150 MHz S11, S12, S22 Graph

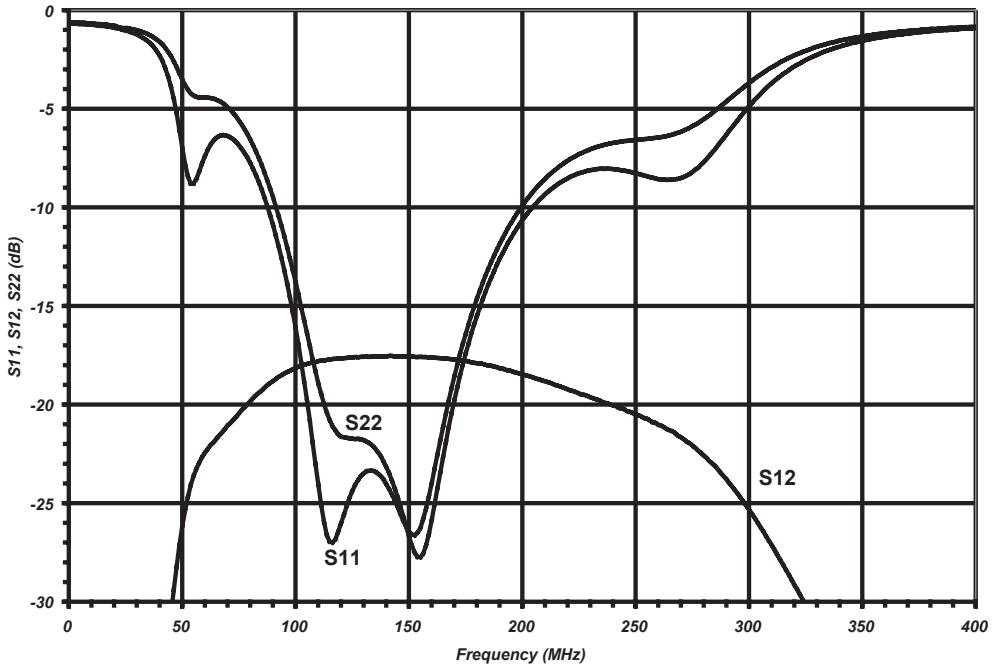
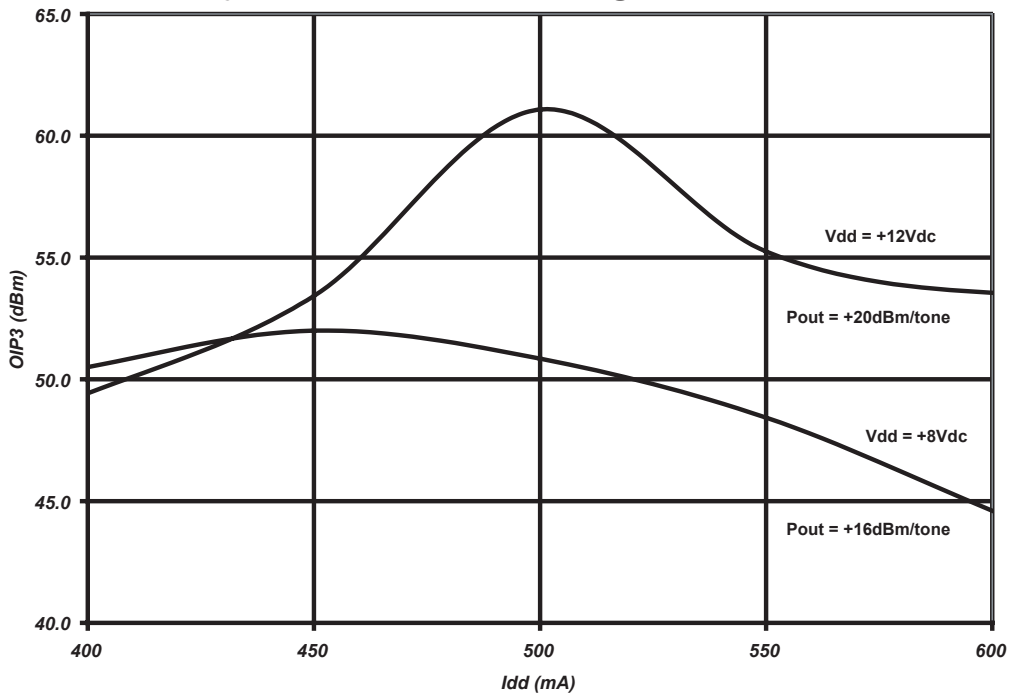


Figure 7: Typical OIP3 (20 dBm Pout) vs IDD @ 12 V (150 MHz)  
 Typical OIP3 (16 dBm Pout) vs IDD @ 8 V (150 MHz)



## ADAPTING THE ACA0861C FOR 50 Ω OPERATION

### PERFORMANCE DATA - 450 MHz

**Table 3: 450 MHz 12 V**

| PARAMETER         | MIN | TYP  | MAX | UNITS |
|-------------------|-----|------|-----|-------|
| Frequency         | 350 | 450  | 500 | MHz   |
| VDD               | -   | 12   | -   | VDC   |
| IDD               | 400 | 475  | 600 | mA    |
| Gain              | -   | 10.5 | -   | dB    |
| Noise Figure      | -   | 3.0  | -   | dB    |
| Output Power      | -   | +20  | -   | dBm   |
| OIP3 <sup>1</sup> | -   | +52  | -   | dBm   |
| P1dB              | -   | +31  | -   | dBm   |

NOTE:

1. Measured using two CW tones at an output power level of +20 dBm per tone.

**Table 4: 450 MHz 8 V**

| PARAMETER         | MIN | TYP  | MAX | UNITS           |
|-------------------|-----|------|-----|-----------------|
| Frequency         | 350 | 450  | 500 | MHz             |
| V <sub>DD</sub>   | -   | 8    | -   | V <sub>DC</sub> |
| I <sub>DD</sub>   | 400 | 425  | 600 | mA              |
| Gain              | -   | 10.5 | -   | dB              |
| Noise Figure      | -   | 3.0  | -   | dB              |
| Output Power      | -   | +16  | -   | dB              |
| OIP3 <sup>1</sup> | -   | +16  | -   | dBm             |
| P1dB              | -   | +28  | -   | dBm             |

NOTE:

1. Measured using two CW tones at an output power level of +16 dBm per tone.

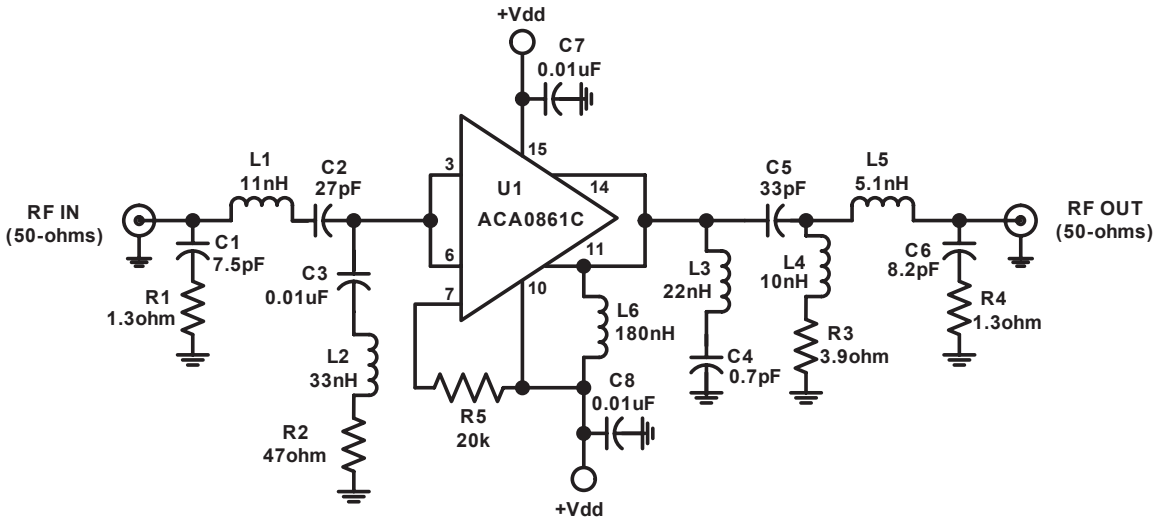


Figure 8: 450 MHz Circuit

Figure 9: 450 MHz S21 Graph

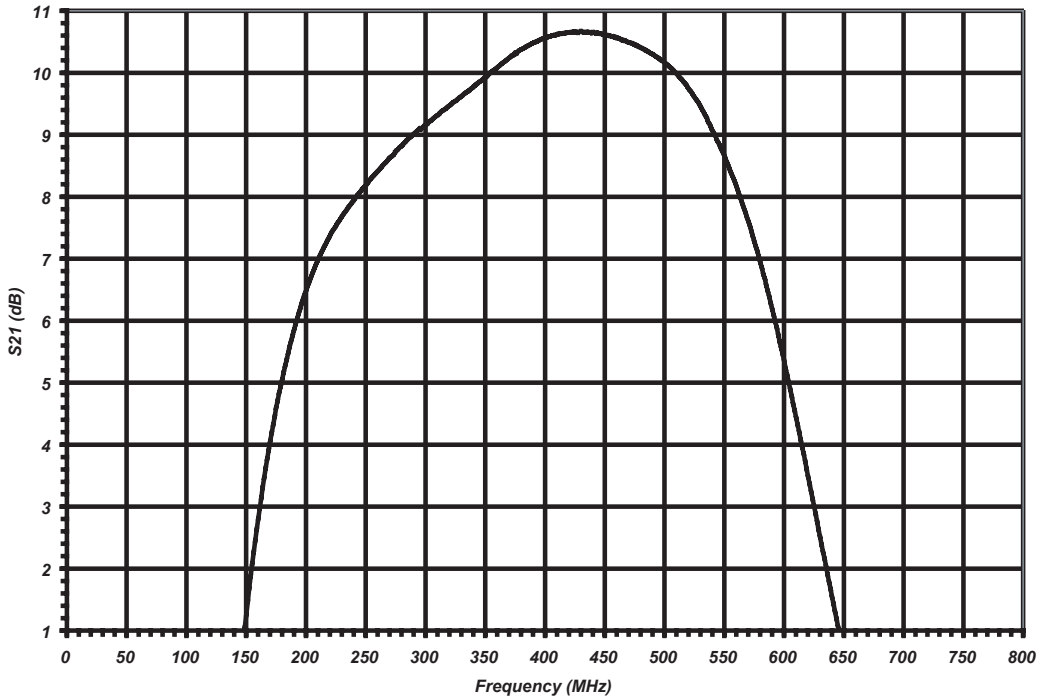


Figure 10: 450 MHz S11, S12, S22 Graph

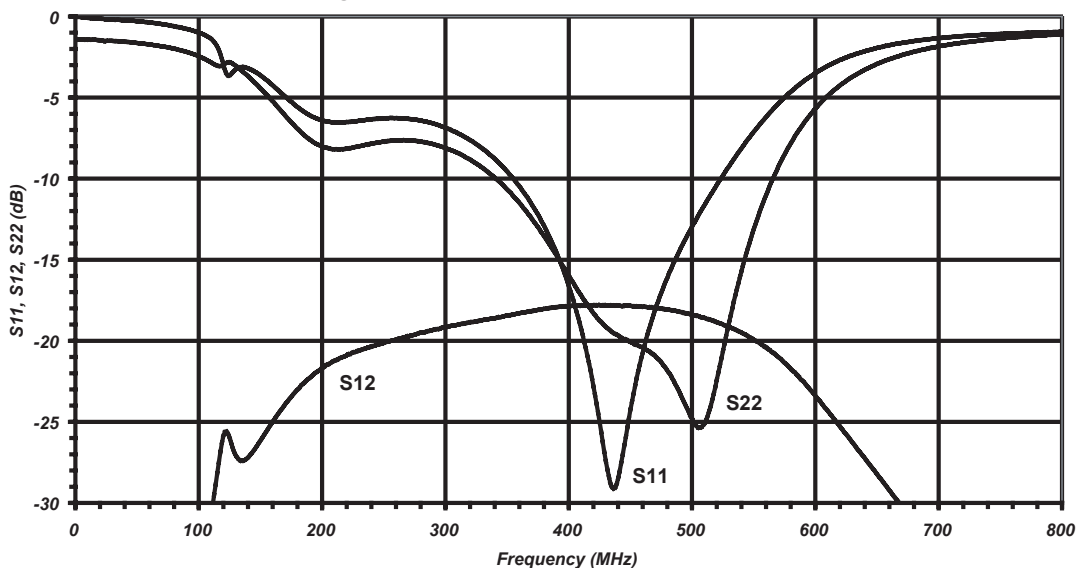


Figure 11: Typical OIP3 (20 dBm P<sub>OUT</sub>) vs I<sub>DD</sub> @ 12 V (450 MHz)  
 Typical OIP3 (16 dBm P<sub>OUT</sub>) vs I<sub>DD</sub> @ 8 V (450 MHz)

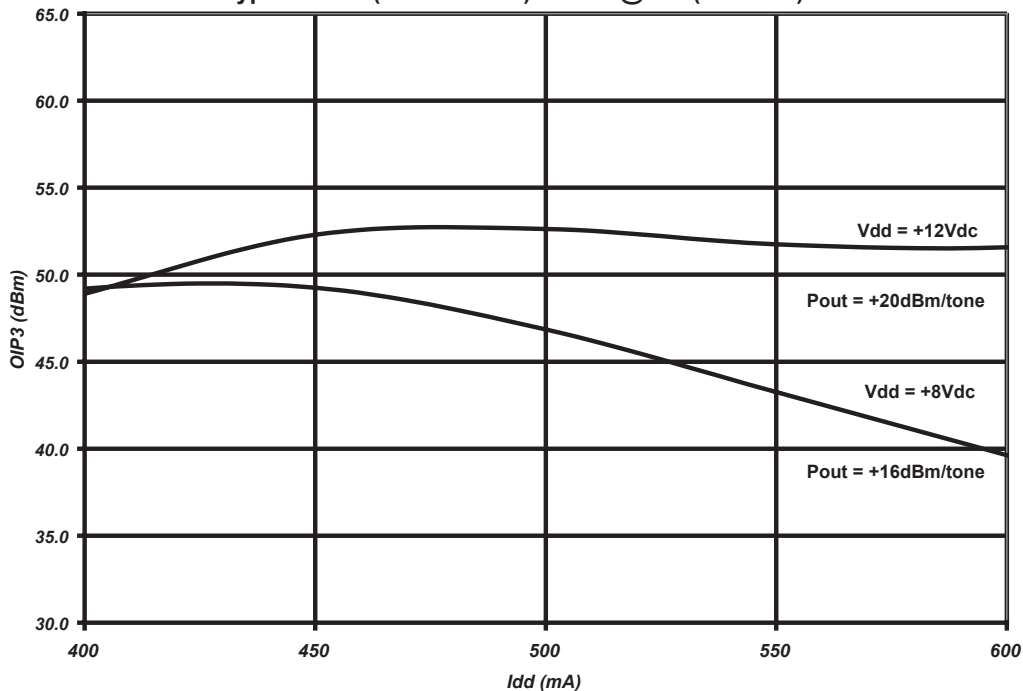


Table 5: 950 MHz 12 V

| PARAMETER         | MIN | TYP   | MAX  | UNITS           |
|-------------------|-----|-------|------|-----------------|
| Frequency         | 850 | 950   | 1150 | MHz             |
| V <sub>DD</sub>   | -   | 12    | -    | V <sub>DC</sub> |
| I <sub>DD</sub>   | 400 | 450   | 500  | mA              |
| Gain              | -   | 10.5  | -    | dB              |
| Noise Figure      | -   | 3.0   | -    | dB              |
| Output Power      | -   | +16   | -    | dBm             |
| OIP3 <sup>1</sup> | -   | +58   | -    | dBm             |
| P1dB              | -   | +26.5 | -    | dBm             |

## NOTES:

1. Measured using two CW tones at an output power level of +16dBm per tone.

Table 6: 950 MHz 8 V

| PERFORMANCE       | MIN | TYP   | MAX  | UNITS           |
|-------------------|-----|-------|------|-----------------|
| Frequency         | 850 | 950   | 1150 | MHz             |
| V <sub>DD</sub>   | -   | 8     | -    | V <sub>DC</sub> |
| I <sub>DD</sub>   | 350 | 400   | 450  | mA              |
| Gain              | -   | 10.5  | -    | dB              |
| Noise Figure      | -   | 3.0   | -    | dB              |
| Output Power      | -   | +13   | -    | dBm             |
| OIP3 <sup>1</sup> | -   | +42   | -    | dBm             |
| P1dB              | -   | +23.5 | -    | dBm             |

## NOTES:

1. Measured using two CW tones at an output power level of +13 dBm per tone.

# ADAPTING THE ACA0861C FOR 50 Ω OPERATION

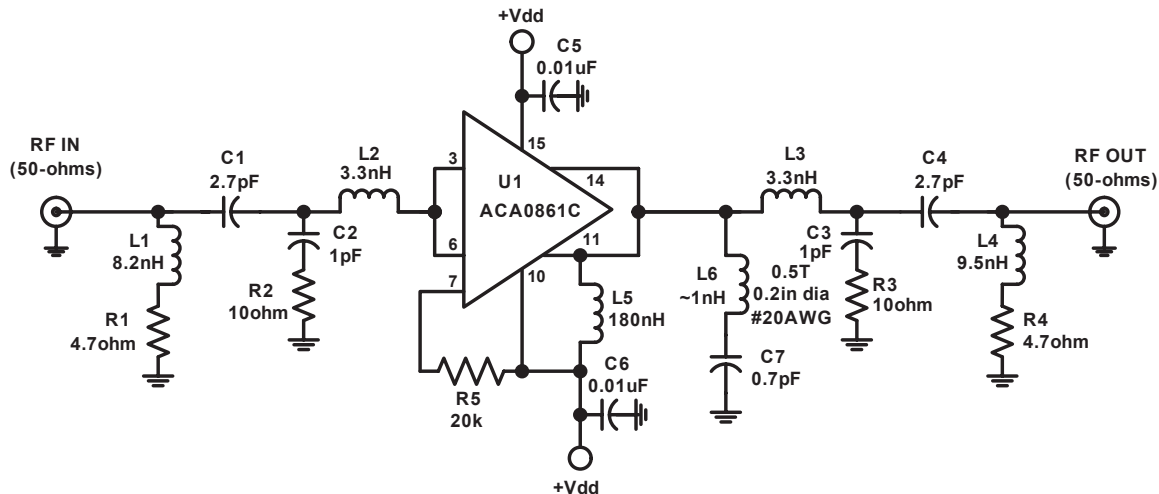


Figure 12: 950 MHz Circuit

Figure 13: 950 MHz S21 Graph

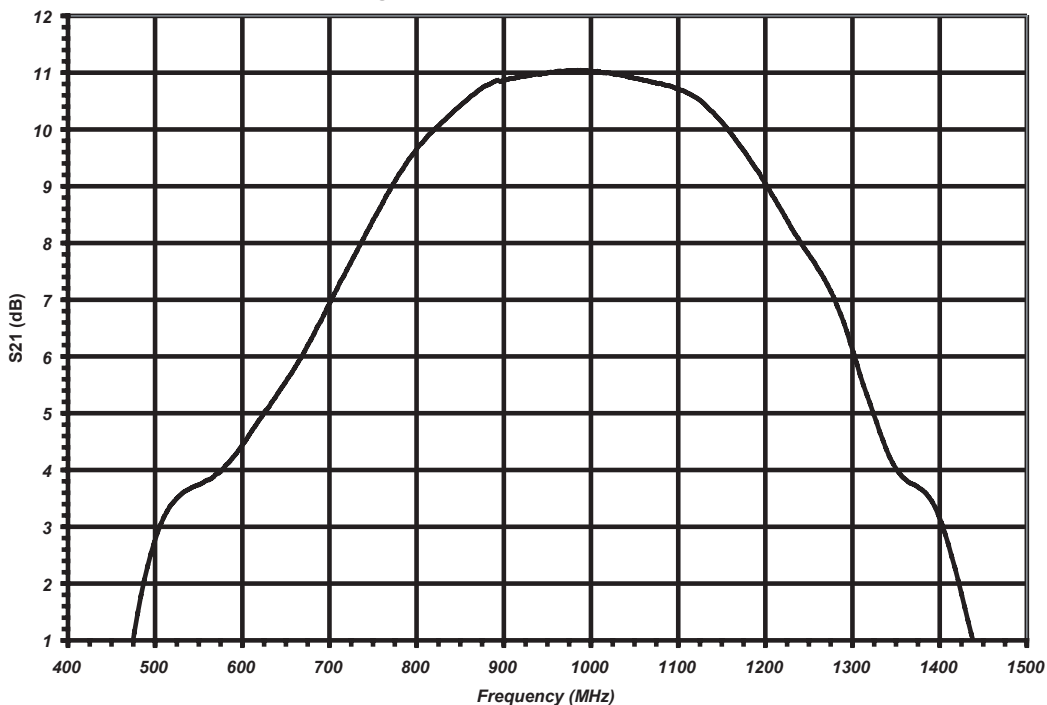


Figure 14: 950 MHz S11, S12, S22 Graph

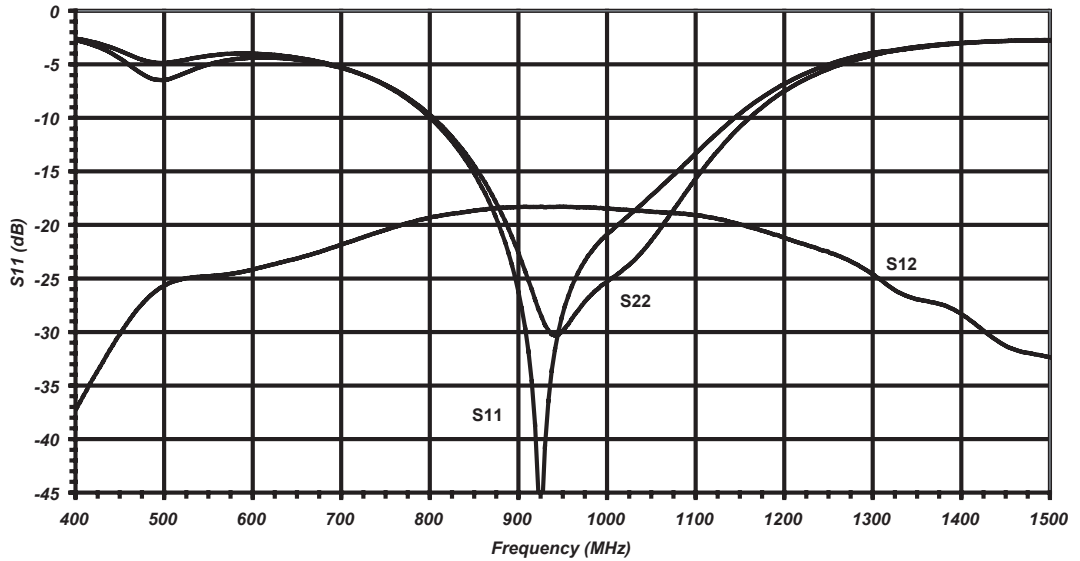
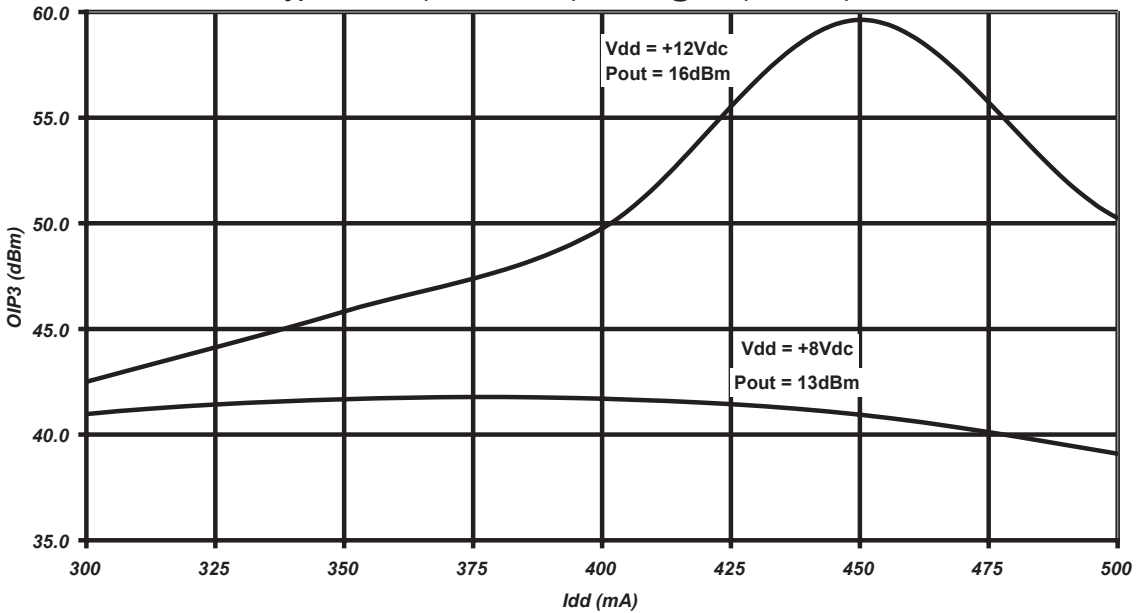


Figure 15: Typical OIP3 (16 dBm P<sub>OUT</sub>) vs IDD @ 12 V (950 MHz)  
 Typical OIP3 (13 dBm P<sub>OUT</sub>) vs IDD @ 8 V (950 MHz)



## ADAPTING THE ACA0861C FOR 50 Ω OPERATION

### Reduced Current Consumption

The total power dissipation may be reduced in exchange for a slight degradation in the linearity performance. Reductions in current have no effect on the Gain (S21). The overall current consumption of the device is controlled by the magnitude of the

voltage across pin #7. The relationship between the  $V_{BIAS}$  and the Current Consumption is depicted in the graph below. The performance is characterized at a nominal  $V_{BIAS}$  of +1.0 V<sub>DC</sub> at 12 V<sub>DD</sub>.

Figure 15: I<sub>DD</sub> vs V<sub>BIAS</sub> @ 8 V & 12 V

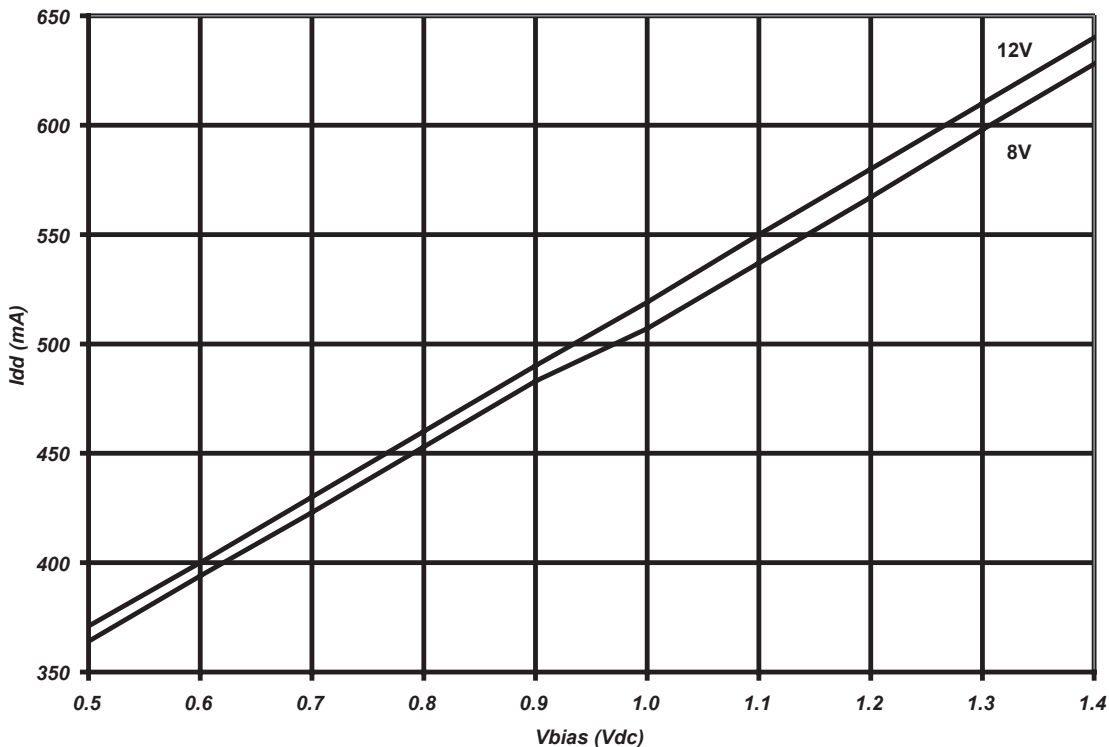
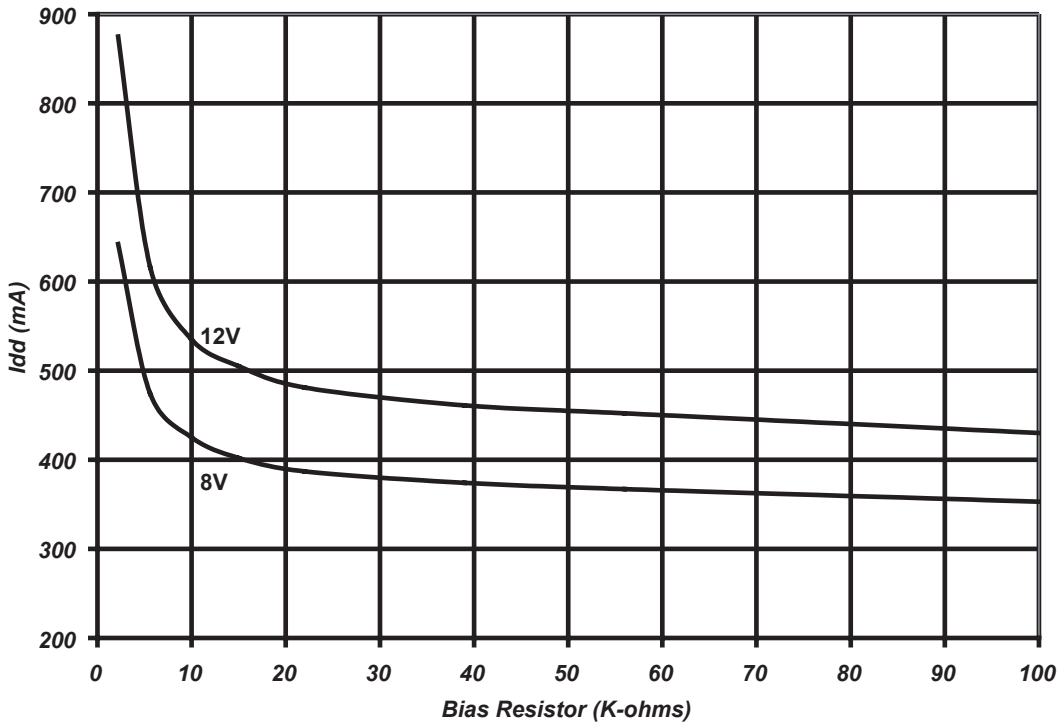


Figure 16: Bias Resistor vs  $I_{DD}$  @ 8 V & 12 V

#### Assembly/Mounting and Thermal Considerations

The ACA0861C, under normal biasing conditions, dissipates approximately 5Watts of power and is capable of dissipating in excess of 8Watts under aggressive biasing. Therefore, proper soldering of the heat slug, located on the bottom surface of the package, is critical. A comprehensive description of the recommended layout, mounting, and thermal considerations is presented in the ANADIGICS Application Note “ACA0861-A,B,C,D 750/860MHz CATV Line Amplifiers”. This document is available for downloading from the ANADIGICS website at:

<http://www.anadigics.com/content/download/323/1338/version/2/file/ACA0861.pdf>



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