

### RELEVANT PRODUCTS

- AND0041R
- AWT6168R

### INTRODUCTION

This power amplifier module supports dual, tri and Quad Band applications for GMSK and 8-PSK modulation schemes using a polar architecture. The module includes an internal reference voltage and integrated power control scheme for use in both GMSK and 8-PSK operations. This facilitates fast and easy production calibration and reduces the number of external components required to complete a power control function. This integrated control loop reduces the development time associated with optimizing loop filters to meet time mask and switching transient requirements, as it is completely self-contained.

The module size is a competitive 7 mm x 7 mm and with the few external components required, it is well suited for a small form factor transmit front-end solution.

### GENERAL DESCRIPTION

The application circuit below shows the relative ease with which this amplifier can be designed into a GSM transmit front-end. All of the RF-ports for this device are internally matched to 50Ω.

The RF-inputs can interface to transmit VCO's with the addition of simple attenuators. These can be used to set the input drive to the PA and is generally good practice to help minimize any possible load pulling effects at the VCO, PA interface. The RF-outputs can interface directly to an antenna switch module to complete the front-end solution.

The logical control inputs, TX\_EN and BS, are both 1.8 V and 3 V logic compliant. The TX\_EN is used to enable the amplifier typically with the TX burst. The BS is used to select which amplifier is enabled.

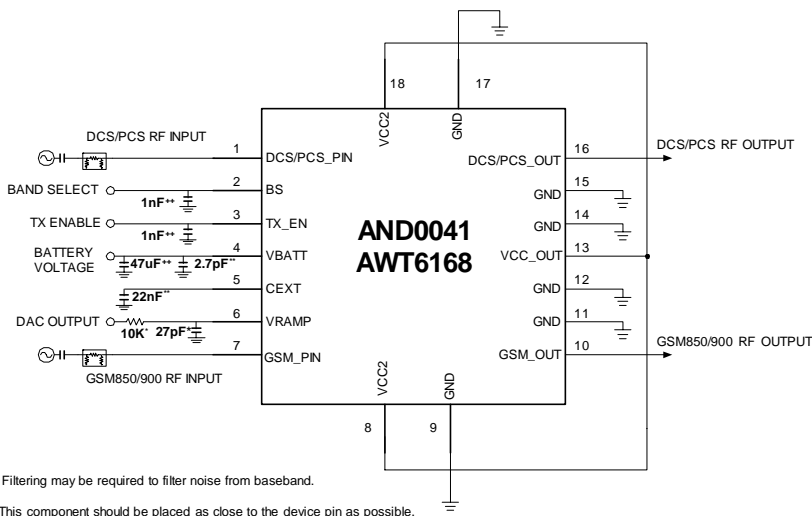


Figure 1: Recommended Application Circuit

# Quad Band/GPRS/Polar EDGE Power Amplifier Module With Integrated Power Control

## POWER CONTROL

The scheme used is a closed loop method that requires only the application of an analog voltage to the  $V_{RAMP}$  pin to set the output power. This can be applied directly from a standard DAC output. The method used does not require any power or current sensing. Setting the  $V_{RAMP}$  voltage, in turn sets the collector voltages of the power amplifiers to a multiple of the  $V_{RAMP}$  voltage using a pre-determined formula. This collector voltage is regulated in a voltage control loop as shown in below. The amplifier's bias is held constant while the collector voltage is adjusted to set the power. The relationship between the output power and collector voltage is described by Equation 1.

$$P_{OUT} (Watts) = \frac{(2 \cdot V_{CC} - V_{SAT})^2}{8 \cdot R_{LOAD}}$$

Equation 1

where  $V_{CC}$ ,  $V_{SAT}$  are the collector voltage and saturation voltage of the transistor respectively. This

expression shows how the power variation due to  $V_{BATT}$  is limited due to voltage control loop.

Under extreme conditions, as the battery voltage degrades, it is important to maintain the control loop bandwidth, so the collector voltage quickly follows  $V_{RAMP}$ . This is done by adjusting  $V_{RAMP}$ , such that:

$$V_{RAMP} \leq 0.38 \cdot V_{BATT} + 0.20 \leq 1.6V$$

Equation 2

The effect of the loop bandwidth slowing can be seen most clearly in the switching transients measurement. This adjustment can be incorporated in the software of the final application, so that performance is enhanced under low voltage conditions. Another advantage of this control scheme is the improved noise performance due to individual stages being held in compression, thus improving the overall receive band noise performance.

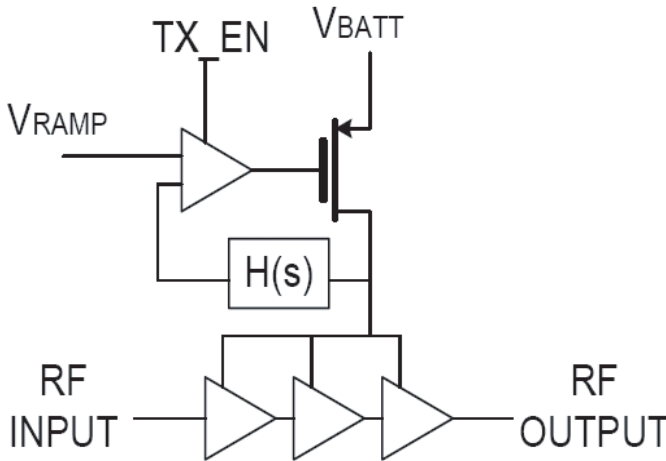
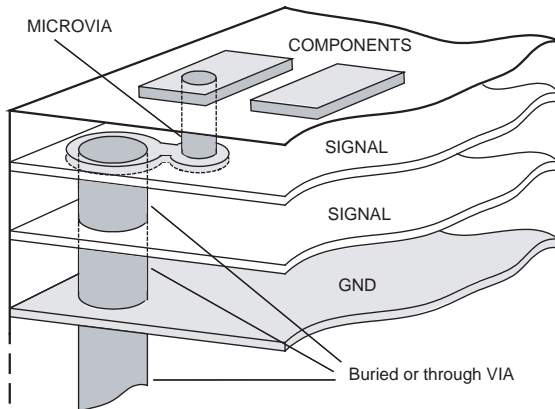


Figure 2: Voltage Control Loop

## DESIGN RECOMMENDATIONS

### 1. RF DECOUPLING

To comply with any potential radiated contribution around the PAM mostly related to PCB design it is good practice to place two RF decoupling ceramic capacitors on  $V_{BATT}$  pin 4 of the AND0041, as close to the PAM as possible. Also, provision should be made to bypass  $V_{BATT}$  at the battery connector with the same level of decoupling. This can be accomplished by placing two ceramic capacitors similar to the ones at  $V_{BATT}$  pin 4 as close as possible to the  $V_{BATT}$  pin of the battery connector. The grounding of any bypass capacitors is critical to achieve the expected improvements. All GND for decoupling capacitors should be connected to the main GND-plane as directly as possible preferably using microvias, see PCB cutout in Figure 3.



**Figure 3: Example of GND Connection from Pad Using Microvia and Buried Via**

The values of the capacitors chosen depend on their location, grounding and physical size. These factors determine the resonant frequency at which the decoupling is most effective. One cap should be optimized for the GSM850/900 band performance, the other for DCS/PCS. The  $V_{BATT}$  line going from the  $V_{BATT}$  connector pin to the AND0041  $V_{BATT}$  pin 4 should be kept as short as possible and preferably shielded inside the PCB between two GND-layers (known as stripline) in order to suppress any possible radiation originating from this line.

### 2. INPUT POWER

The part operates over the 0 to 5 dBm range and has been optimized for best typical performance at

3 dBm. ANADIGICS recommends a series capacitor and resistive attenuator to be placed between the VCO and PAM. Some transceiver designs require a capacitor between the VCO-output of the chipset and the resistive attenuator on the input of the PAM because the VCO-output has a DC-offset. The attenuator helps prevent load pulling of the VCO by further improving the return loss and also gives the flexibility to optimize the input drive to the PAM, which will depend on the transceiver output power and losses prior to the PAM. In order to avoid potential problems of strong RF-signals radiating or coupling to other parts of the circuit, we suggest that the attenuator is placed as close to the transceiver chip VCO-output as possible.

### 3. MATCHING BETWEEN PA AND ANTENNA SWITCH MODULE (ASM)

Provision should be made for matching the ASM to 50 ohms. Though the ASM usually specifies 50 ohms impedance, the actual impedance on the PCB is dependent on the transmission lines at the PA interface, and any vias and buried layer routing. This is rarely 50 ohms. A T-network or  $\pi$ -network is recommended for the matching as this gives sufficient flexibility. The component values used for the matching are dependent on the impedance presented by the ASM used.

### 4. ANALOG RAMP VOLTAGE INPUT

At the  $V_{RAMP}$  input pin 6 an analog voltage to set the output power can be applied directly from a standard DAC-output. In order to smoothen this DAC-output staircase shaped signal, it is recommended to make provision for an RC-filter. The values for this filtering depend on DAC bit-resolution and sample rate.

### 5. CONTROL VOLTAGE OUTPUT & INPUT

The control voltage output  $V_{CC\_OUT}$  pin 13 must be directly connected to the two voltage control inputs  $V_{CC2}$  pins 8 & 18, which are used for the internal low and high-band pre-amplifier stages, respectively. It is recommended to route these connections with a V-shaped track. The trace width used should be at least 0.4 mm due to the peak DC-current in these connections.

### 6. PCB LAYOUT GROUNDING

To have the best performance good grounding is crucial. “Local ground planes” only connected to the board GND plane using a few microvias is not adequate. All GND planes must be connected to the main GND layer (one designated inner layer of the PCB) using a lot of through vias. Besides being the reference for the all RF- and other signals, the GND plane is also used to distribute the heat dissipated by the PA and should therefore by sufficient size and with many through vias to spread the heat to other copper layers. In order to establish a good ground connection for the PA, it is necessary to assign an area on the first inner layer to GND. Microvias will go from the large GND pad under the PA to area on the inner layer and buried or through vias will go the rest of the way to the ground plane in the center of the board, see Figure 4.

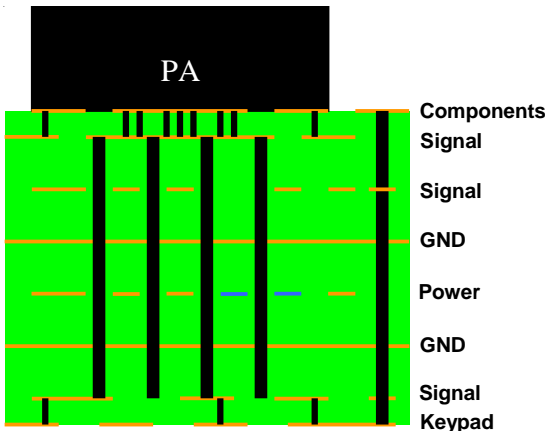


Figure 4: Example of PCB Stack-up with Microvias from Top and Bottom Layers, Buried Vias from Layers 2 to 7, and through Vias from Layers 1 to 8

For more information regarding GND underneath the PAM, please refer to the “Package Outline” chapter and the “Soldering Guidelines for Module PCB Mounting - Application Note”. Generally it is good practice to establish shielding around the PAM. For the shielding to be effective, a good GND-connection is also required. Therefore a lot of vias should be used, where the shielding - whether it is metallized plastic or a traditional shielding can - is attached to the PCB surface, see Figure 5.

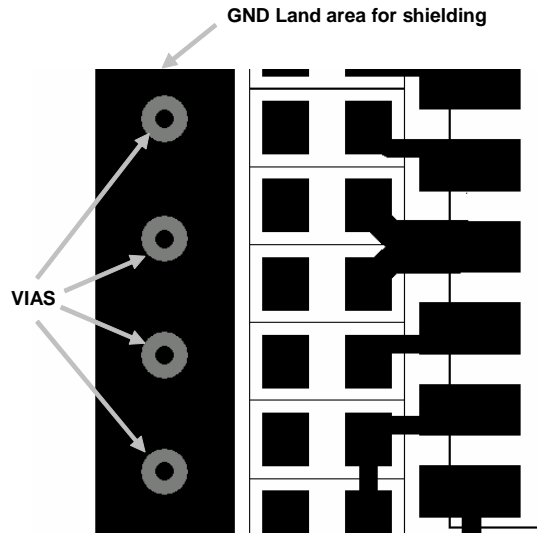


Figure 5: Example of Via Placement at Shielding Landpattern Close to PA

### 7. RF TRACKS

Keep RF tracks as short as possible and with as few corners and bends as possible. Make openings in the ground plane on the layer just under all 50 Ω pads on the PAM and the FEM (Front End Module) or ASM (Antenna Switch Module). The short distance between the component layer and the first inner layer is very small compared to the pad size. This means that the pads terminate the transmission line in low impedance much different from that of the track. The result of this is mismatch, which again can result in up to a couple of dB loss of signal. As a rule of thumb, ANADIGICS normally uses a clearance around microstrips and striplines of at least the same width as that of the track, i.e. if the track width is 12 mil or 0.3 mm, the clearance on both sides of the track to any copper area is also 12 mil or 0.3 mm.

Generally keep reference clock signals, digital signals or analogue I and Q signals away from RF-tracks, V<sub>BATT</sub> and the V<sub>CC\_OUT</sub> to V<sub>CC2</sub> connections. Make sure that these different signal connections are not running directly underneath or above RF-tracks, V<sub>BATT</sub>, V<sub>CC\_OUT</sub> & V<sub>CC2</sub> without a proper distance or GND in between.

## SETUP RECOMMENDATIONS

### 1. TIMING

In order to meet the ETSI specified GSM power time template and switching transients, the sequence of events outlined in Figure 6 is recommended. The timing on BS is not critical; it just needs to be enabled and settled prior to TX\_EN going high (approx. 2  $\mu$ s). The PA “forward isolation 1” parameter and the

ASM isolation ensure the template is met outside the burst. The PA “forward isolation 2” parameter ensures the time template is met during the burst with sufficient margin. The timing of the TX\_EN is critical to ensure the application has sufficient margin for meeting the burst timing requirement.

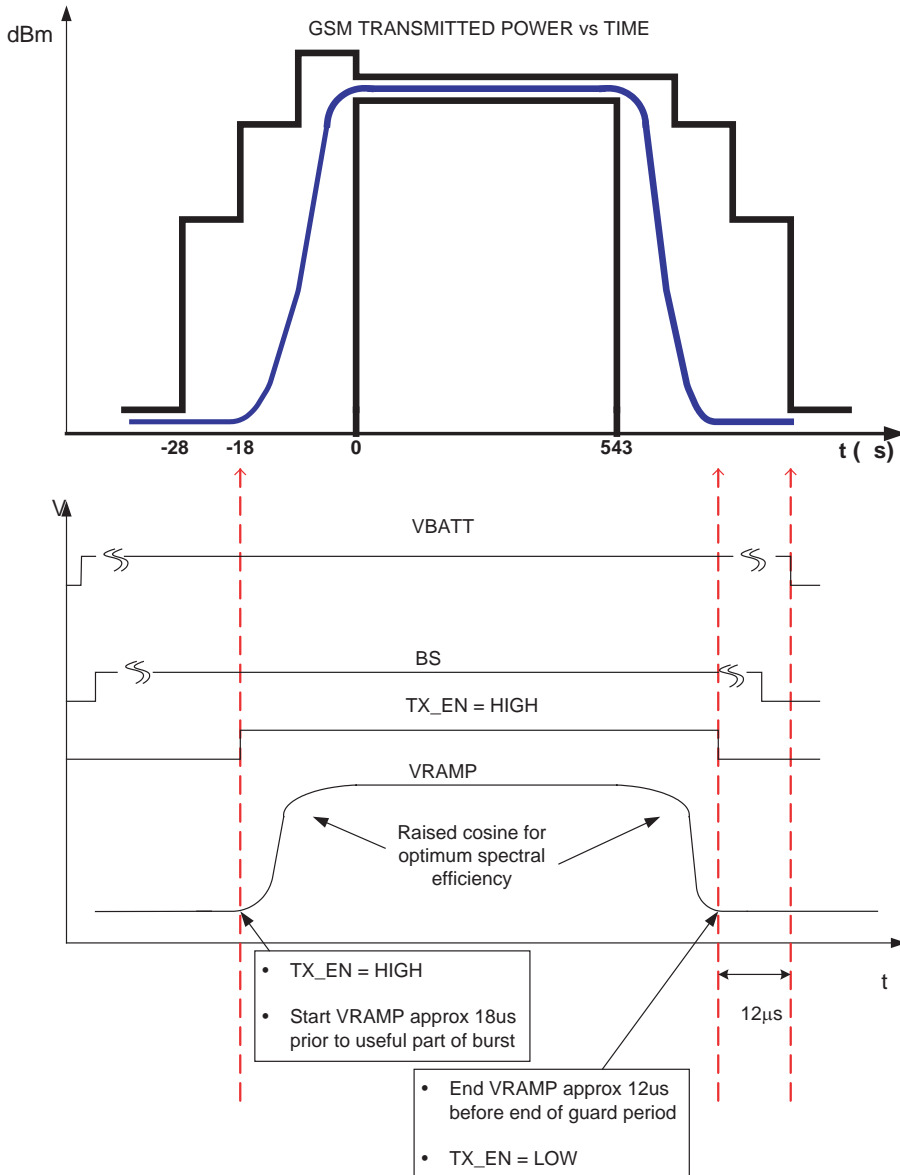


Figure 6: Timing Recommendations

## Quad Band/GPRS/Polar EDGE Power Amplifier Module With Integrated Power Control

The change in the power ramping profile could possible conflict with the timing of the PA. Since the signals like TX\_EN are usually used to improve the isolation, it can be quite close to the V<sub>RAMP</sub> ramping signal. If one of the control signals for instance controlling the ASM conflicts with the V<sub>RAMP</sub> signal, it usually results in a very poor switching spectrum performance. In order to verify this, all the control signals for ASM, TX\_EN, BS, etc. should be compared with the V<sub>RAMP</sub> profile using an oscilloscope. The timing can affect the switching spectrum and the isolation. In Figure 7 and Figure 8 the yellow line [1] is the V<sub>RAMP</sub> signal and the blue line [2] is TX\_EN and the figures shows an example of how logic signals should be kept clear of the power ramping signal V<sub>RAMP</sub>.

ramping with regard to switching spectrum when developing a new platform. This is usually not a complicated task, and can be done manually in a few hours. The power ramping affects switching spectrum, and have to meet the Power Time Template specified by ETSI. Generally the ramp profile should be as close as possible to a raised cosine waveform. In Figure 9 & 10 is an example of a smooth shaped power ramping profile resulting in good switching spectrum performance, see Figure 11. The example is based on measurement results from a radio demo platform based on an ANADIGICS PAM and a standard GSM tranceiver. The baseband signals for this platform are provided by ANADIGICS baseband emulator.

### 2. POWER RAMPING

Since different PAMs have different control characteristics, it is necessary to optimize the power

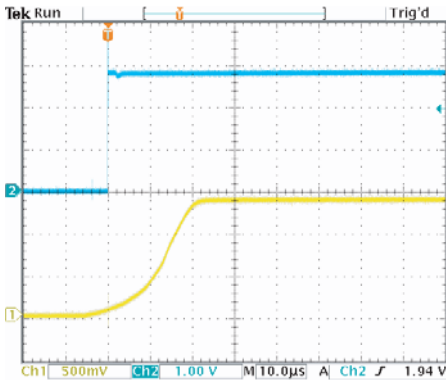


Figure 7: Close in of the Timing With a Proper Distance Between the Logic TX\_EN Signal and the Analogue Power Ramping Signal V<sub>RAMP</sub>

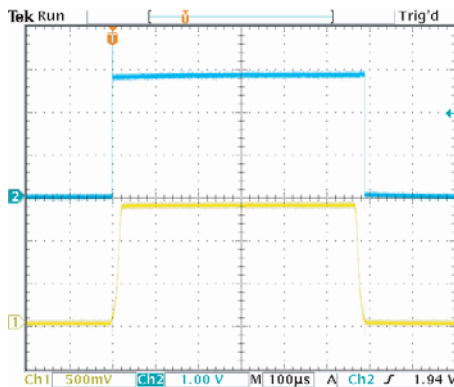


Figure 8: Total Timing Period of TX\_EN & V<sub>RAMP</sub> With a Proper Distance Between the Logic TX\_EN Signal and the Analogue Power Ramping Signal V<sub>RAMP</sub>

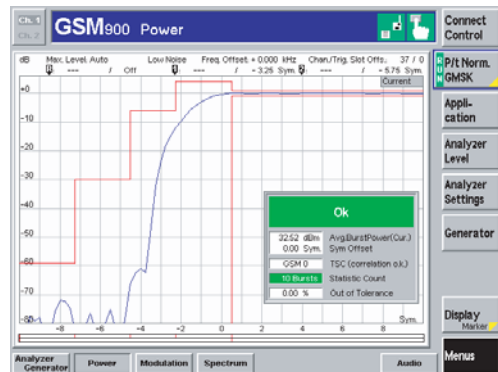


Figure 9: Rising Edge of a Smooth Power Ramping Profile Example Resulting in Good Switching Spectrum

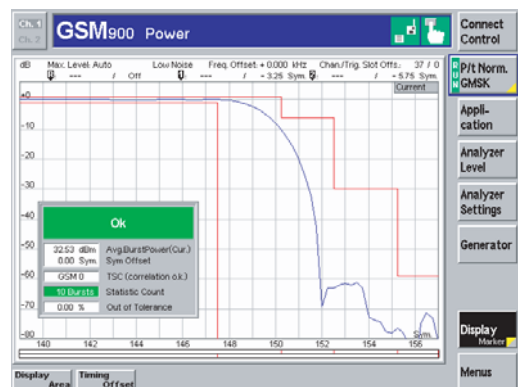


Figure 10: Falling Edge of a Smooth Power Ramping Profile Example Resulting in Good Switching Spectrum

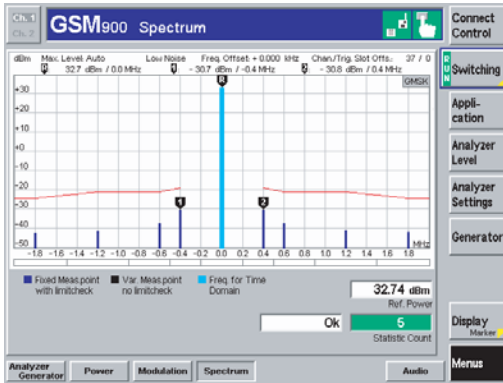


Figure 11: Corresponding Switching Spectrum Result from the Total Power Ramping Profile Shown in Figures 9 and 10

### 3. OUTPUT MATCHING OF THE PAM

Different PAMs will have different load contours. This means that they, in order to function at optimum performance, need to have the output matching

circuitry tuned. The way to do this is by using the load contours provided by ANADIGICS and a network analyzer and then tune the matching network on the PA output toward the desired performance. The optimum matching network will usually be a compromise between output power, current consumption, and conducted harmonics. In most cases, 50 Ω is the best choice. In extreme cases, the switching spectrum can be affected if a poor matching solution is selected. Thereby it limits the output power to the point of conflict with the ETSI specifications and forces the PA close to saturation.

### EVALUATION BOARD

The evaluation board is a multilayer board using GETEK substrate, which is similar to FR4, but has a more controlled dielectric constant. The board thickness is 1.57 mm. All the routing is on the top layer (1) of a 4 layer board with a distance of 0.36 mm to the ground plane, which is on layer 2. All RF routing has been sized to present a 50 Ω impedance.

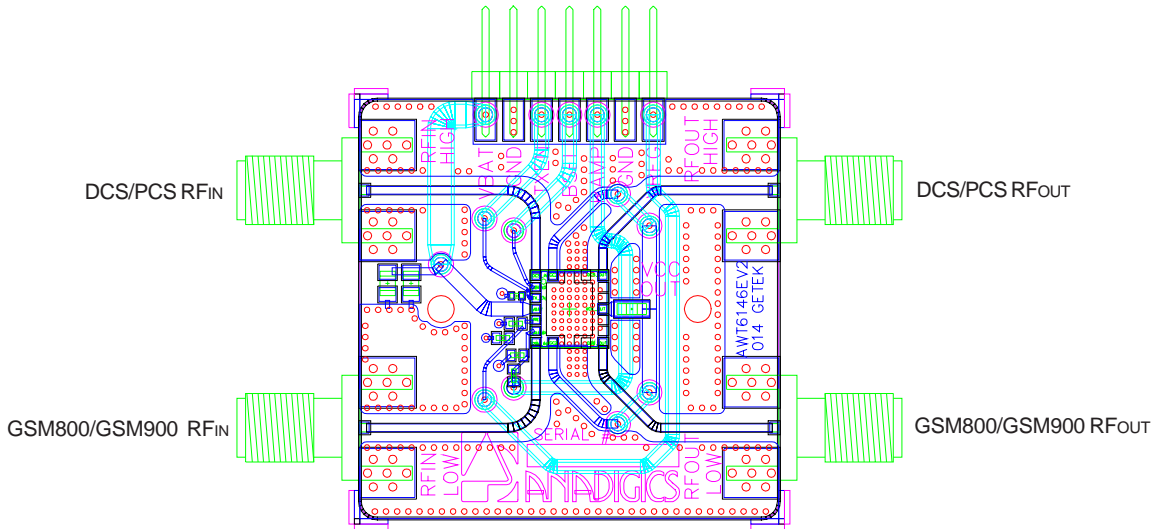
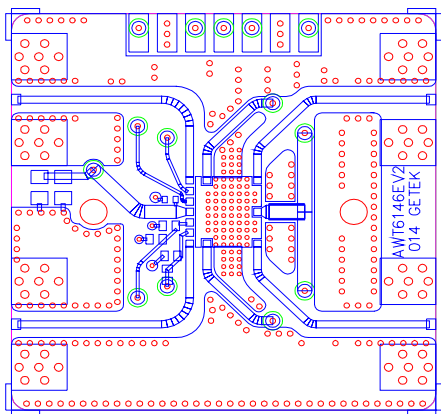
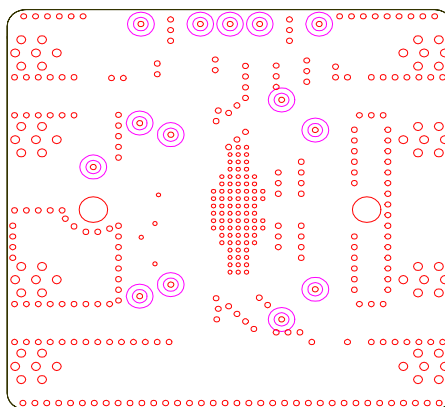


Figure 12: AND0041 Evaluation Board

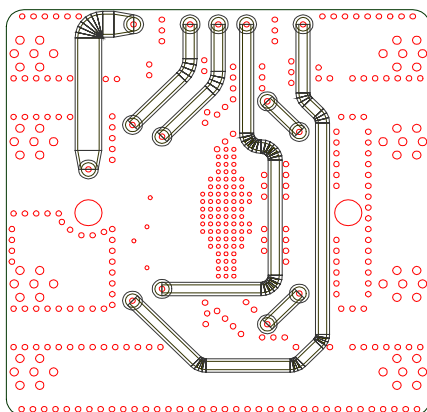
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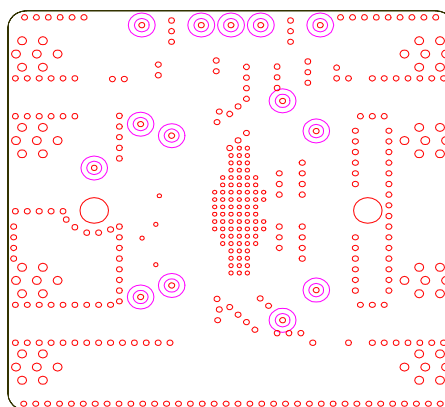
**Layer 1**



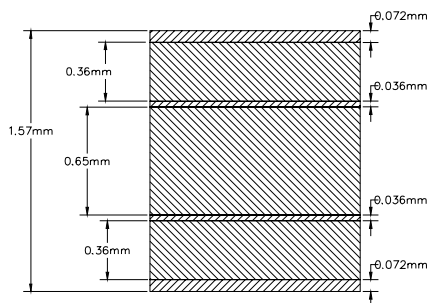
**Layer 2**



**Layer 3**



**Layer 4**



## LEGEND

-  CONDUCTOR LAYER
-  DIELECTRIC LAYER

**Figure 13: Evaluation Board Layout and Structure**

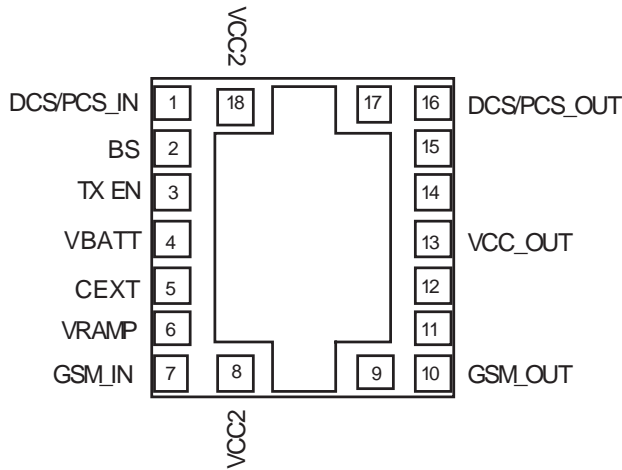


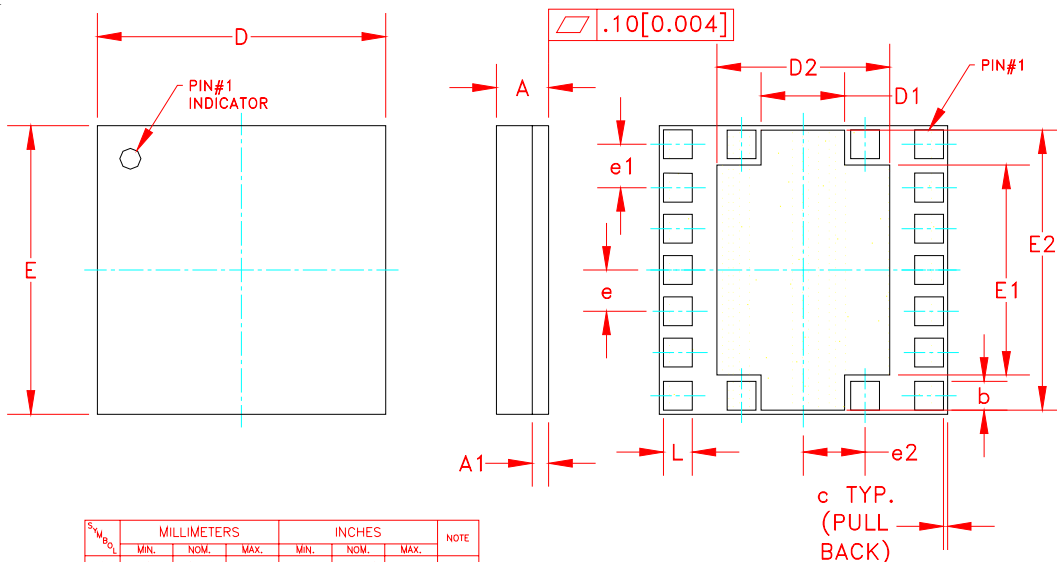
Figure 14: Pinout (X-Ray View)

Table 1: Pin Description

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	DCS/PCS_IN	DCS/PCS RF Input	10	GSM_OUT	GSM850/900 RF Output
2	BS	Band Select Logic Input	11	GND	Ground
3	TX_EN	TX Enable Logic Input	12	GND	Ground
4	VBATT	Battery Supply Connection	13	VCC_OUT	Control Voltage Output Which Must be Connected to Vcc2, no decoupling
5	C_EXT	Bypass	14	GND	Ground
6	V_RAMP	Analog Signal Used to Control the Output Power	15	GND	Ground
7	GSM_IN	GSM850/900 RF Input	16	DCS/PCS_OUT	DCS/PCS RF Output
8	VCC2	Vcc Control Input for GSM850/900 Pre-amplifier	17	GND	Ground
9	GND	Ground	18	VCC2	Vcc Control Input for DCS/PCS Pre-amplifier

# Quad Band/GPRS/Polar EDGE Power Amplifier Module With Integrated Power Control

## PACKAGE OUTLINE



SYMBOL	MILLIMETERS			INCHES			NOTE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
A	1.16	1.31	1.46	0.045	0.051	0.057	-
A1	-	0.30	-	-	0.012	-	-
b	0.67	-	0.73	0.026	-	0.028	-
c	-	0.10	-	-	0.004	-	-
D	6.88	7.00	7.12	0.270	0.275	0.280	-
D1	1.99	-	2.11	0.078	-	0.083	-
D2	4.14	-	4.26	0.163	-	0.168	-
E	6.88	7.00	7.12	0.270	0.275	0.280	-
E1	5.07	-	5.13	0.199	-	0.202	-
E2	6.74	-	6.86	0.265	-	0.270	-
e	-	1.00	-	-	0.039	-	8X
e1	-	1.05	-	-	0.041	-	4X
e2	-	1.50	-	-	0.059	-	4X
L	0.67	-	0.73	0.026	-	0.028	-

### NOTES:

1. CONTROLLING DIMENSIONS: MILLIMETERS
2. UNLESS SPECIFIED TOLERANCE=±0.076[0.003].
3. PADS (INCLUDING CENTER) SHOWN UNIFORM SIZE FOR REFERENCE ONLY. ACTUAL PAD SIZE AND LOCATION WILL VARY WITHIN MIN. AND MAX. DIMENSIONS ACCORDING TO SPECIFIC LAMINATE DESIGN.

Figure 16: Package Outline

**NOTES**



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