

**Figure 2: Single-Stage Amp (#2) Configuration**

Note:

Amp Stage #1 and Attenuator Stage disabled.

**CURRENT CONTROL**

The current drawn by each amplifier is controlled by adjusting the value of the resistor,  $R_s$ , that is placed at pin 11 for Amplifier #1 and at pin 25 for Amplifier #2. Electrical performance is characterized for  $R_s$  values of 0-ohms and 3.9-ohms.

**TYPICAL PERFORMANCE**

Each amplifier, when operated in accordance with the schematic diagrams shown above, yields a typical Gain, Noise Figure, and Harmonic Linearity performance profile as outlined in the tables below.

**Table 1: Gain vs. Frequency vs.  $R_s$**

FREQUENCY (MHz)	Gain(dB)	
	$R_s = 0$ ohms	$R_s = 3.9$ ohms
10	16.32	16.14
20	16.19	16.02
30	16.15	15.99
40	16.08	15.94
50	16.06	15.91
75	15.73	15.60
100	15.42	15.30
125	14.96	14.86
150	14.46	14.45
175	14.15	14.07
200	13.76	13.68
225	13.32	13.25
250	12.88	12.83

Table 2: Gain vs. Frequency vs. Rs

FREQUENCY (MHz)	Gain(dB)	
	Rs = 0 ohms	Rs = 3.9 ohms
10	16.32	16.14
20	16.19	16.02
30	16.15	15.99
40	16.08	15.94
50	16.06	15.91
75	15.73	15.60
100	15.42	15.30
125	14.96	14.86
150	14.46	14.45
175	14.15	14.07
200	13.76	13.68
225	13.32	13.25
250	12.88	12.83

Table 3: Harmonics vs Frequency (Pout = +58dBmV)

FREQUENCY (MHz)	Linearity - Harmonics (dBc)			
	Rs = 0 ohms I = 104mA		Rs = 3.9 ohms I = 77mA	
	X2	X3	X2	X3
5	-58.4	-66.0	-49.3	-63.0
10	-59.5	-67.0	-49.7	-63.0
12	-60.0	-70.3	-50.3	-69.3
20	-58.8	-69.7	-49.3	-62.0
35	-59.0	-67.3	-52.3	-63.8

S-parameters

The input return-loss (S11), forward gain (S21), reverse isolation (S12), and output return-loss (S22) are plotted in the following four graphs presented below.

Figure 3: Input Return Loss (S11) Amplifier Stage 1 or 2

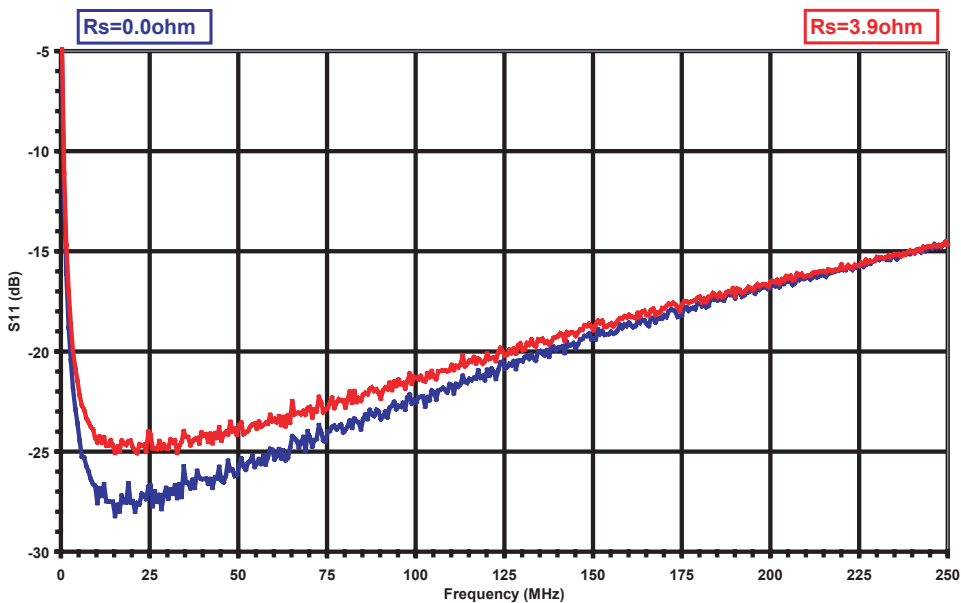


Figure 4: Gain (dB) (S21) Amplifier Stage 1 or 2

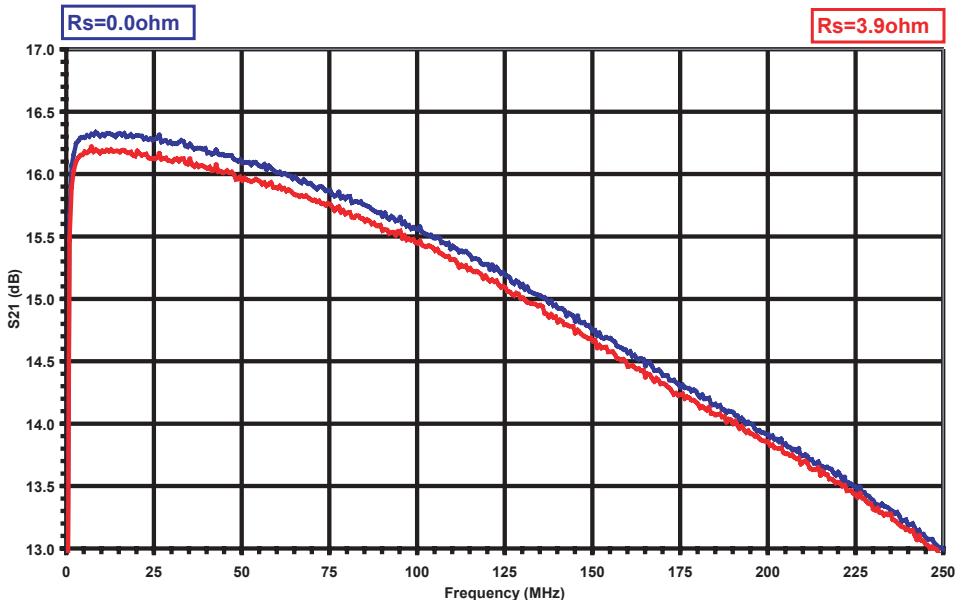


Figure 5: Reverse Isolation (S12) Amplifier Stage 1 or 2

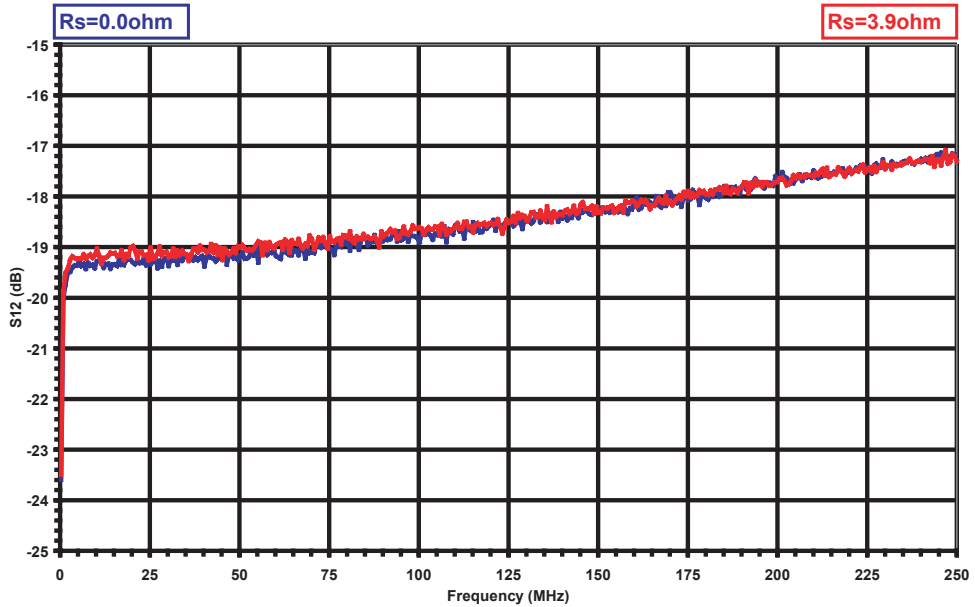
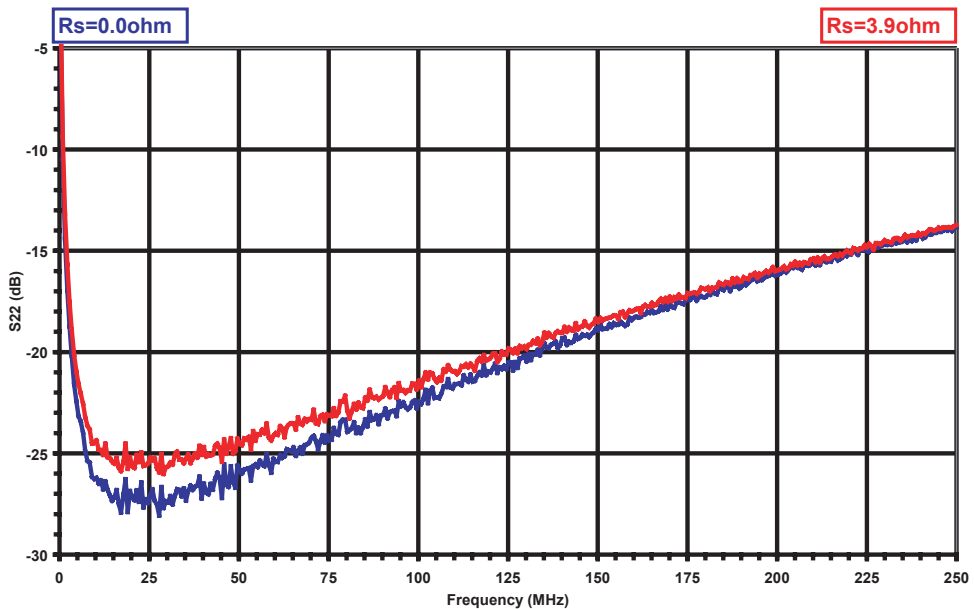


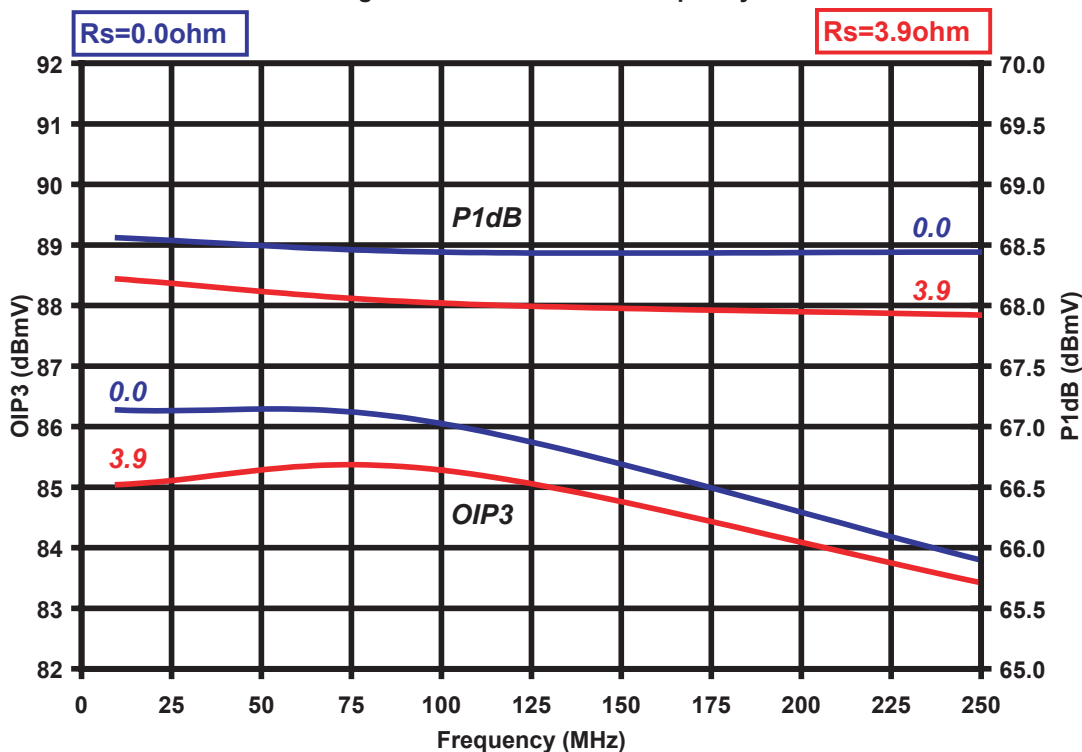
Figure 6: Output Return Loss (S22) Amplifier Stage 1 or 2



**Linearity**

Plots of the third order output intercept (OIP3) point and the gain compression (P1dB) point as a function of  $R_s$  are depicted below. The testing conditions are published in the ARA05050 Data Sheet.

Figure 7: OIP3 & P1dB vs Frequency

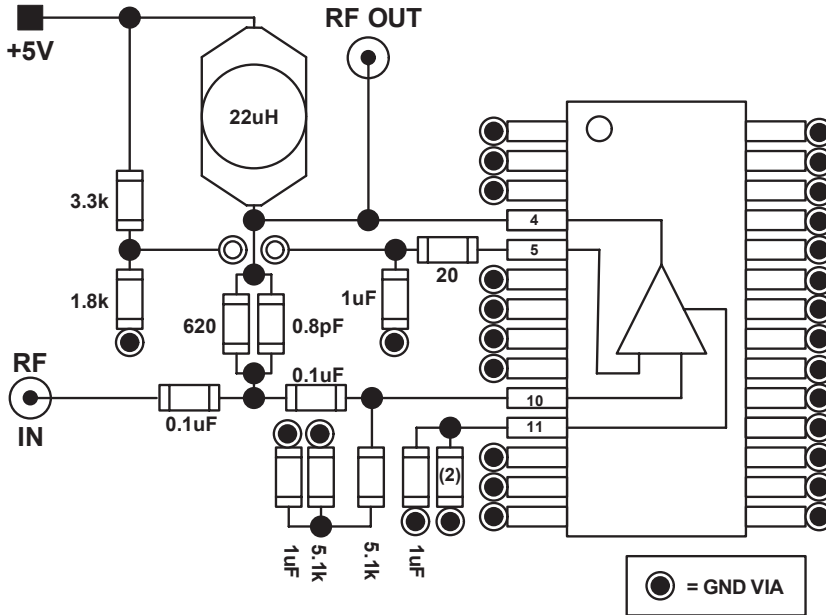


**COMPONENT PLACEMENT**

For best performance, it is suggested that the components be oriented nominally as shown in diagrams 1 & 2 below. Each component is dimensioned as “0603” with the exception of the 22uH inductor. Standard, low-cost double-sided pcb construction utilizing FR4 dielectric is adequate for use with this IC. It is recommended to fabricate the bottom layer as a solid ground plane devoid of DC and signal paths. The one exception that is permissible is the cross-over that can be seen immediately adjacent to the 22uH inductor element.

The general orientation of the components is based upon the layout of the ARA05050 Evaluation Test Fixture. The original pcb file defining the Test Fixture artwork is available from ANADIGICS upon request.

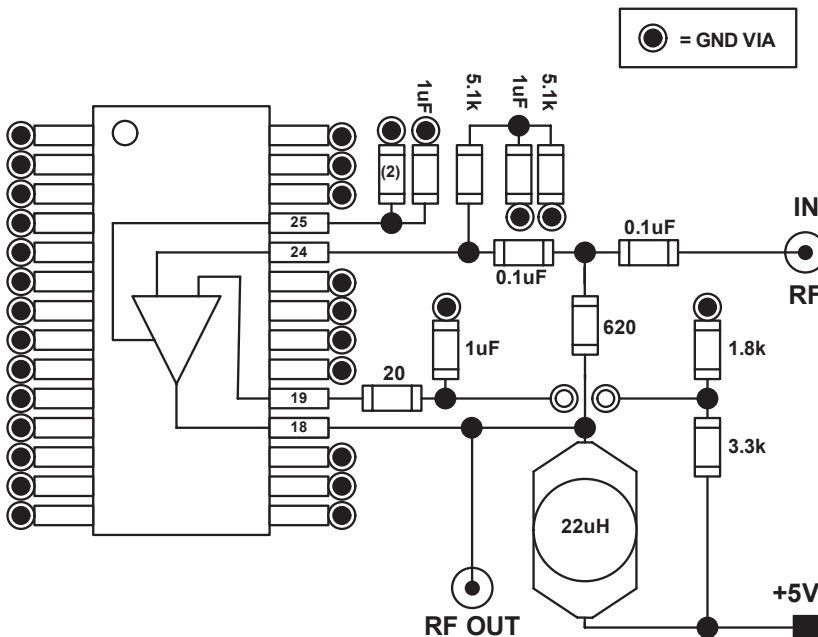
The pcb layout is designed to enable the operation of both stages simultaneously along with the Attenuator section. However, the user is encouraged to import this pcb file and to modify it in accordance with the particular needs of his system architecture.



**Figure 8: Single-Stage Amp #1 Components**

Notes:

1. Amp Stage #2 and Attenuator Stage disabled.
- (2) 0.0 or 3.9 Ohms.



**Figure 9: Single-Stage Amp #2 Components**

Notes:

1. Amp Stage #1 and Attenuator Stage disabled.
- (2) 0.0 or 3.9 Ohms.

## ARA05050 for Low Frequency Amplifier Applications

### PCB LAYOUT

Thermal management and RF parasitics must be considered during the pcb layout process.

#### Thermal Considerations

The ARA05050 dissipates a maximum total power of 1.3Watts when both amplifier stages are biased using values for  $R_s$  of 0-ohms. Maximum MTF is achieved by minimizing the temperature of the active devices in the circuit die. A heat slug is incorporated into the bottom of the IC package to provide a low-resistance path for efficient thermal energy evacuation. Adequate heat sinking must be applied to the heat slug for optimal thermal management.

A metalized pad with via holes to ground as shown in Figure 3 is recommended. The heat slug is soldered to this pad during the assembly process. It is also recommended that the solder mask outline depicted in Figure 4 be adopted for ease of solderability.

#### RF Layout Considerations

The ARA05050 is designed to drive a 75-ohm single-ended load. The layout of the PCB affects performance at RF frequencies.

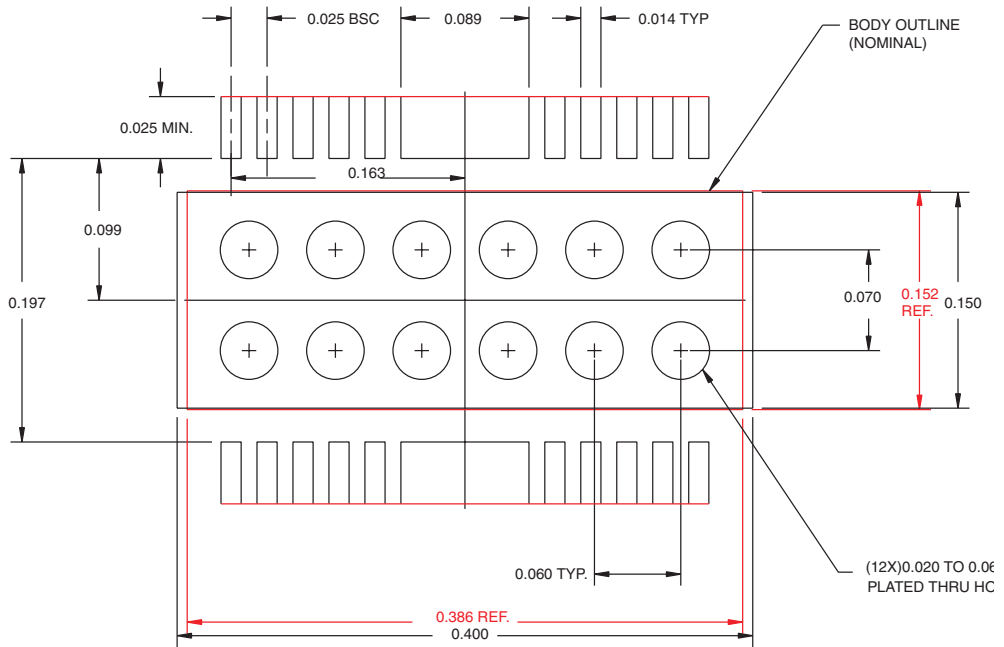
The quality of the ground connections is a critical item in an RF layout. These ground connections must be low-impedance and be as short as possible. Specify 0.030-inch diameter via-holes to ground and locate them as close to the ground pins as possible.

Other non-ground related aspects must be considered. For example, traces connecting IC pins to their respective components should have a low value of impedance. A few additional special considerations are listed below:

Pins 5 & 19: The 1uF capacitor and the 20ohm chip resistor should be as close as possible to the IC pins.

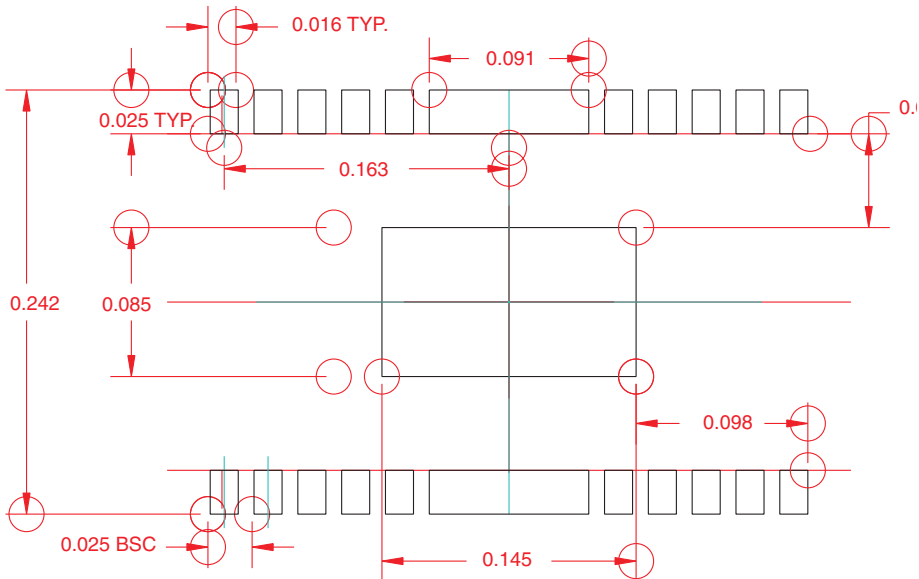
Pins 11 & 25: The 1uF bypass capacitor should be close to the pin.

All bypass capacitors on the Vdd lines should be located as close as possible to the 22uH inductors.



\*Dimensions are in inches [Millimeters]

**Figure 10: PC Board Layout for Heatsink**



\*Dimensions are in inches [Millimeters]

**Figure 11: Solder Mask Outline**



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