ANADIGICS

Application Note

Thermal Design for AWM6423

Rev 0

RELEVANT PRODUCTS

- AWM6423
- AWM6422

OVERVIEW

ANADIGICS' AWM6423 WiMAX Power Amplifier is a high performance device that delivers exceptional linearity and efficiency at high output power levels. The device operates over the voltage supply range of +2.9Vdc to +4.2Vdc, and its output power handling capabilities increase as the supply voltage is raised towards the high end of this range. At higher output powers, thermal considerations need to be taken into account in order to maintain high levels of device reliability.

This application note addresses thermal design considerations for the AWM6423 by first measuring the junction-to-case thermal characteristics of the device, and performing a case-to-ambient thermal analysis. Thermal design examples and guidelines are then offered for specific applications and circuit boards used.

THERMAL CHARACTERIZATION AND ANALYSIS

Thermal characterizations of the AWM6423 were performed on an open cavity device (no mold compound) that was mounted to an evaluation board. The AWM6423 is a class A/B amplifier, and thus requires RF drive in order for the output stage to be fully operational. The thermal characterizations were performed using a dc bias of 3.3V and a 2.6GHz CW (no modulation) signal of various power levels, in order to produce total currents between 300mA and 550mA in steps of 50mA. This procedure was used to validate the consistency of the junction-case thermal resistance measured.

In performing the thermal scans, the evaluation board temperature was raised until the case temperature (Tc) of the device was 75°C, as measured at the bottom of the package. The peak thermal rise was detected at the third (output) amplification stage, and this rise was used to derive the junction-case thermal resistance (θ_{J-C}) for the device.

Table 1 shows the thermal analysis, based on the thermal scan results for the device operating at 3.3V. The data presents the derivations of the junction-case thermal resistance (θ_{J-C}) and demonstrates the consistency of the θ_{J-C}, which averages 24.7 °C/W under multiple drive conditions.

Table 2 shows the derivation of the junction-case temperatures (T_{J-C}) when Tc is at 25°C and 85°C. The typical value for T_{J-C} as presented was calculated based a typical output stage gain of 11dB, an average θ_{J-C} of 24.7°C/W, and an output power of +23.5dBm (nominal) at a 3.3Vdc supply voltage.

Table 1: Thermal Analysis of an AWM6423 Device Operating at 3.3V under Multiple Drive Conditions

	Thermal characterizations under drive conditions						
	#1	#2	#3	#4	#5	#6	Unit
DC Analysis							
Total current @ 3.3Vdc	300	350	400	450	500	550	mA
Typical currents (1st and 2nd stage) Icc1 + Icc2 (pin1)	60	60	60	60	60	60	mA
Typical current at output stage Icc3 (pin12)	240	290	340	390	440	490	mA
Typical dc power dissipation at the output stage (P3)	0.792	0.957	1.122	1.287	1.452	1.617	W

Table 1: Thermal Analysis of an AWM6423 Device Operating at 3.3V under Multiple Drive Conditions (continued)

Measured Tj at output stage	91.3	94.5	96.4	97.7	98.6	99.3	°C
Tc	75						°C
Temperature rise measured	16.3	19.5	21.4	22.7	23.6	24.3	°C
RF Analysis							
RF output power (Prf-out)	22.05	23.21	24.77	26.08	27.13	27.95	dBm
	0.160	0.209	0.300	0.406	0.516	0.624	W
Typical RF gain of the output stage	11						dB
RF input power at the output stage (Prf-in3)	11.05	12.21	13.77	15.08	16.13	16.95	dBm
	12.74	16.63	23.82	32.21	41.02	46.55	mW
Junction-case Thermal Resistance Analysis							
Power dissipation (P3 + Prf-in3 - Prf-out)	0.644	0.764	0.846	0.914	0.977	1.043	W
Junction-case thermal resistance (θ_{J-C})	25.3	25.51	25.3	24.8	24.2	23.3	°C/W

The example calculation below is for the AWM6423 device operating at 25°C:

Power Dissipated in the Output Stage: Pdiss = Pin – Pout
= (Vcc*Icc3) + RFin3 – RFout = (3.3 * 0.280) + 17.78*10-3 - 0.224 = 0.718W

Thermal rise of junction for the packaged device = Pdiss * θ_{J-C} = 0.718 * 24.7 = 17.74°C

Calculated Junction-Case Temperature with case at 25°C = 25 + 17.74 = 42.7°C

Table 2: Derivation of AWM6423 Junction-Case Temperatures

Case Temperature	25	85	°C
Total Current @ 3.3V (typical)	340	352	mA
Output Stage Current @ 3.3V (typical)	280	292	mA
Output Stage Power Dissipation (typical)	0.718	0.758	W
Temperature Rise calculated using avg. θ_{J-C} of 24.7°C/W	17.74	18.72	°C
calculated Junction-Case Temperature T_{J-C}	**42.7**	**103.7**	**°C**

PRINTED CIRCUIT BOARD THERMAL DESIGN CONSIDERATIONS

In general, it is essential to keep the junction temperature of the device as low as possible to ensure long operating life. This can be accomplished by providing good thermal relief and adequate heat sinking. When mounted to a printed circuit board (PCB), the delta between the device case temperature and the ambient temperature will be determined by several factors; board thickness and number of layers, copper plating thickness, size and number of via holes placed beneath the device package ground area, the PCB layout, the method of attachment of the PCB to the heat sink as well as the design of the heat sink. For typical applications, it is recommended to maximize the number of vias placed below the package ground area.

ANADIGICS' standard AWM6423 evaluation board (EVB) is fabricated using double sided Rogers R3003 PCB material which has a dielectric constant of 3.38, dielectric thickness of 0.008" (0.2mm), and copper thickness of 0.0021" (0.054mm).

Table 3 shows the derivation of the junction-ambient temperature (T_{J-A}) based on the standard AWM6423 EVB operating at 3.3V and 4.2V with output powers of +23.5dBm and +25dBm, respectively. The junction-case data is based on the device thermal characterizations as previously calculated.

The AWM6423 is packaged in a 4.5mm x 4.5mm laminate based module with a backside ground pad of an area of 2.05mm x 4.3mm (0.081" x 0.169"). This ground pad provides RF, DC, and thermal ground for the package. Using vias that are fabricated with 0.012" (0.3mm) and 0.010" (0.25mm) diameter drilled and finished-hole dimensions, respectively, it is possible to place approximately 28 vias of a 4 x 7 pattern beneath the ground pad area of the package.

The thermal resistance of a single copper via (not solder filled) can be calculated as:

$$\theta_{VIA} = L / (\sigma * \pi(Ro^2 - (Ro - Rpl))$$

For a via path length L = 0.254mm, with drilled hole radius Ro = 0.15mm, copper plating Rpl = 0.036mm, and copper thermal conductivity σ = 0.39W/mm°C, the thermal resistance of each via is 21.7°C/W. Therefore, the thermal resistance of the PCB ground pattern (θ_{PCB}) beneath the device ground pad is approximately 0.775°C/W for the 28 copper plated vias. For solder-filled vias, the thermal resistance of each via is 18.4°C/W. Thus, the θ_{PCB} will be 0.657°C/W for 28 solder-filled vias.

Table 3: Derivation of Junction-Ambient Temperatures with Respect to AWM6423 Evaluation Board Using Different Drive and Signal Conditions

	V_{CC} = 3.3V P_{OUT} = 23.5dBm	V_{CC} = 4.2V P_{OUT} = 25dBm	Unit
Total current (typical)	340	370	mA
Output Stage Current (typica)	280	310	mA
Delta between the device case temperature and ambient temperature when device is mounted to an evaluation board. (Device powered up with 100% duty cycle)	32	37	°C
θ_{J-C} (avererage)	24.7	24.7	°C
Output Stage Pdiss @ T_A = 25°C	0.718	1.011	W
Output Stage T_{J-A} @ T_A= 25°C	74.74	86.97	°C
Output Stage Pdiss @ T_A = 85°C	0.758	1.063	W
Output Stage T_{J-A} @T_A = 85°C	135.72	148.26	°C

ADDITIONAL MANUFACTURING SUGGESTIONS

Refer to ANADIGICS' AN-0003 for additional information on soldering and manufacturing.

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