

### RELEVANT PRODUCTS

- AWT6222

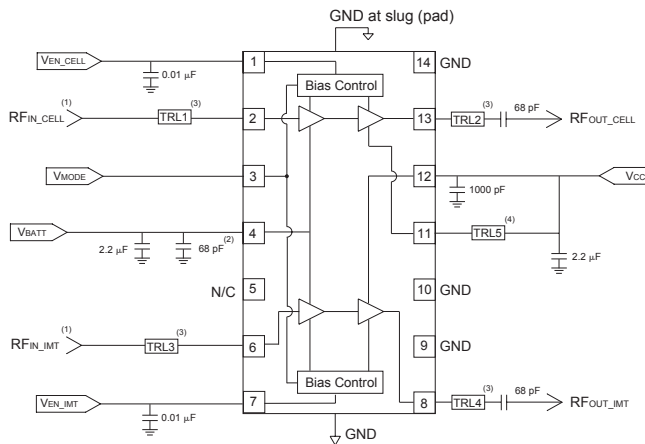
### GENERAL DESCRIPTION

This ANADIGICS 3 mm x 5 mm hetero-junction bipolar transistor (HBT) power amplifier module is designed for Tri-band WCDMA Cellular/JCell/IMT handsets with operating frequency bands from 824 MHz to 849 MHz (Cellular) 830 MHz to 840 MHz (JCell) and 1920 MHz to 1980 MHz (IMT). The amplifier inputs and outputs

are matched to provide optimum performance in a 50 Ω system, and minimal external components are required for proper RF bypassing.

**Table 1: Module Pin Description**

PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	V <sub>EN_CELL</sub>	Enable Voltage for Cell Band	8	RF <sub>OUT_IMT</sub>	RF Output for IMT Band
2	RF <sub>IN_CELL</sub>	RF Input for Cell Band	9	GND	Ground
3	V <sub>MODE1</sub>	Mode Control Voltage1	10	GND	Ground
4	V <sub>BATT</sub>	Battery Voltage	11	V <sub>CC</sub> A	Supply Voltage A
6	V <sub>MODE2</sub> (N/C)	No Connection	12	V <sub>CC</sub>	Supply Voltage
6	V <sub>CC</sub>	RF Input for IMT Band	13	RF <sub>OUT_CELL</sub>	RF Output for Cell Band
7	V <sub>EN_IMT</sub>	Enable Voltage for IMT Band	14	GND	Ground



Note:

(1) Add blocking cap if DC voltage is present on input pin.

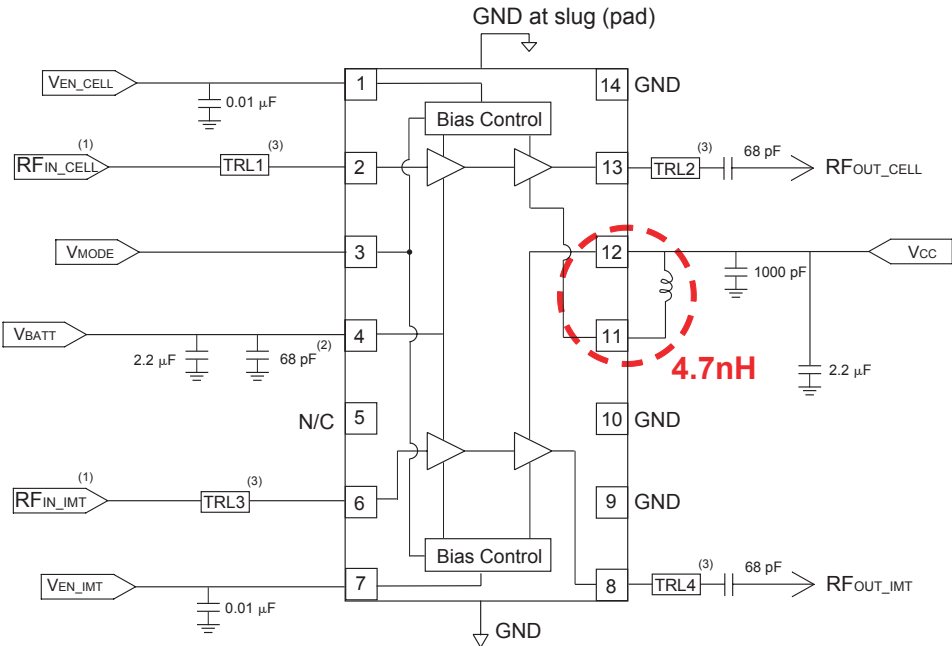
(2) 68 pF cap should be placed as close as possible to Pin 4.

(3) TRL should be short and of 50 Ω characteristic impedance.

(4) TRL 5 should be as long as possible (minimum of 0.1 λ at 800 MHz) and capable of handling 750 mA current.

Optional 4.7 nH Inductor may be substituted.

**Figure 1: Application Schematic**

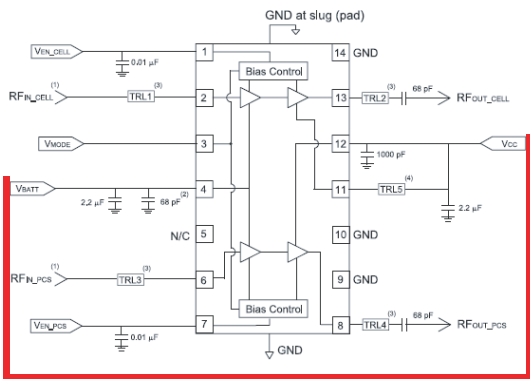


**Figure 2: Dual PA secondary method using Inductor w/o TRL5**

Notes:

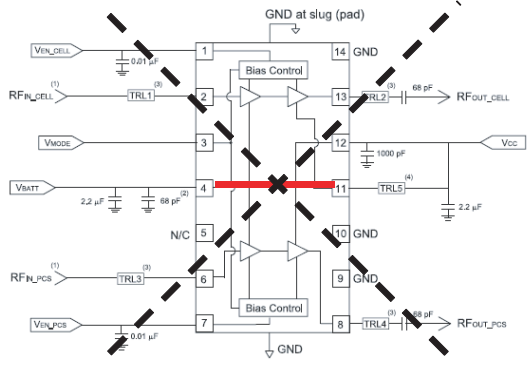
1. Add 4.7nH Inductor across pins 11 & 12
2. Fine tune CELL band PA output matching on your board

**Recommended for PCB Layout**



For better isolation between VBATT and Vcc lines, route as shown above, with a Min. 13mm trace length

**Not recommended for PCB Layout**

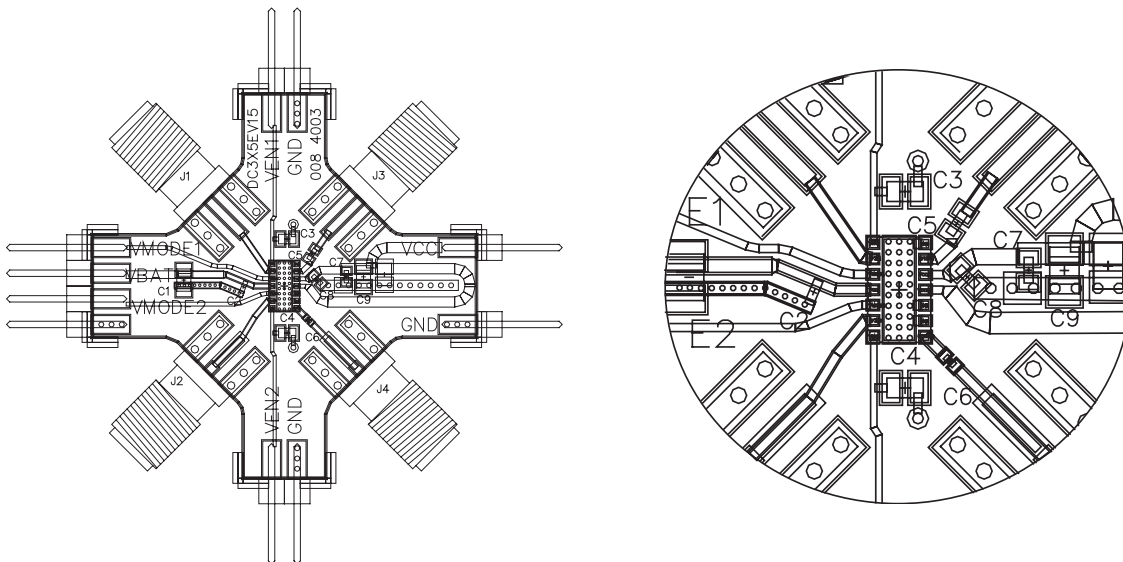


Do not route VBATT and Vcc lines directly as pictured above. There will not be enough isolation between the two

**Figure 3: Dual PA VBATT and Vcc lines connection for isolation**

**EVALUATION BOARD**

The evaluation board, shown in Figure 2, was designed on ROGERS (R04003) material with 8 mils thickness.



**Figure 4: Evaluation Board Layout**

*Notes:*

1. Copper trace width is 20.6 mils.
2. Relative dielectric constant is 3.38 at 1 GHz.
3. Dielectric thickness is 8.0 mils.

**Table 2: Evaluation Board Parts List**

DESCRIPTION	VALUE	SIZE	MANUFACTURER	MANUFACTURER'S P/N (Qty.)	DIGIKEY CROSS REFERENCE
C1, C9	2.2 $\mu$ F	805	KEMET	C0805C225K9RACTU (1)	399-4936-1-ND
C2, C5, C6	68 pF	402	Panasonic	ECJ-0EC1H680J (2)	PCC680CQCT
C3, C4	0.01 $\mu$ F	603	Panasonic	ECJ-1VB1H103K (2)	PCC1784CT-ND
C7	1000 pF	402	Panasonic	ECJ-0EB1C102K (1)	PCC102BQCT
C8	DO NOT INSTALL				
J1, J2, J3, J4			Johnson	142-0711-821 (4)	J629-ND

*Notes:*

(1) Output Power at antenna port of the phone board should not exceed the power level specified on the data sheet (PA Max. output power - Front-end loss). All VSWR value at PA output port toward the antenna port should be lower than 8:1 under 29 dBm Cellular (28.5 dBm IMT) *P<sub>out</sub>* condition, and lower than 5:1 in the absolute maximum RF output power (31.5 dBm Cellular, 31 dBm IMT) condition.

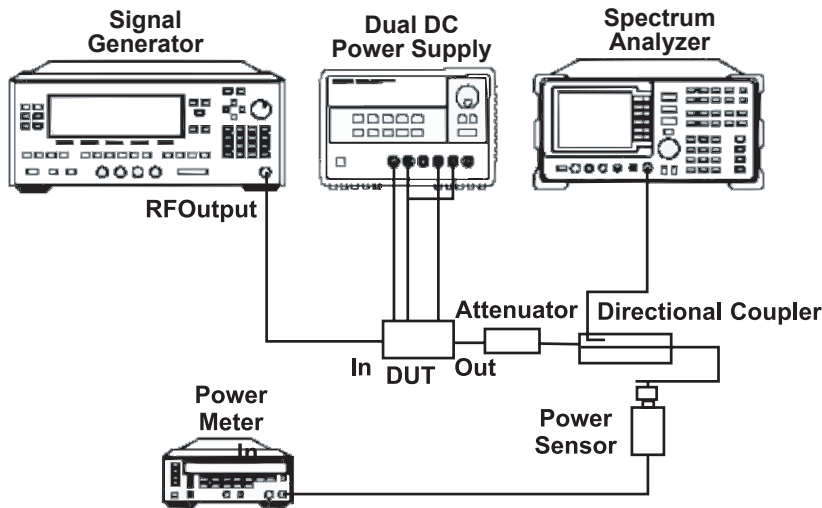


Figure 5: Test Setup Diagram

*Test Setup Notes:*

1. **Figure 3** shows minimum equipment required for proper power amplifier operation.
2. Depending upon the power sensor, 10 to 20 dB attenuator is sufficient to prevent overloading of the power meter or the spectrum analyzer.

**Test Equipment**

The following test equipment is recommended for testing of WCDMA/IMT evaluation boards.

- One RF WCDMA signal generator capable of delivering at least +5 dBm of output power at the operating frequency band (Agilent E4438C).
- One RF power meter capable of measuring up to +30 dBm at the operating frequency band (Agilent E4419B).
- One RF power sensor capable of measuring RF power in the range from -50 dBm to +30 dBm at the operating frequency band (Agilent 4419B).
- One RF spectrum analyzer capable of measuring ACP in operating frequency band and covering up to the 3-rd harmonic of the highest frequency in band (Rohde & Schwarz FSP).
- One DC power supply capable of 4-multi-channels delivering 1.5 A at +4 V and 500 mA at +3 V(Agilent 6624A)
- One SMA 10 dB attenuator capable of handling 2 watts.

*Notes: WCDMA 3GPP 32-03-00, uplink, DPCCH + DP-DCH.*

**Test Setup**

1. Set DC power supply to +3.4 V (for  $V_{BATT}$  and  $V_{CC}$ ), to +2.4 V (for  $V_{EN}$ ), and to 0 V (for  $V_{MODE1}$ ).
2. Set power meter measured frequency to 836 MHz for Cellular band (835 MHz for JCellular),(1950 MHz for IMT band) and its calibration factor to correspond to the set frequency.
3. Set power meter offset value equal to the total loss of the attenuator, directional coupler, and connecting cables.
4. Set spectrum analyzer center frequency to 836 MHz for Cellular band (835 MHz for JCellular),(1950 MHz for IMT band and enable WCDMA(3GPP) measuring personality.
5. Select and enable WCDMA digital signal on the signal generator.
6. Set signal generator frequency to 836 MHz for Cellular band (835 MHz for JCellular),(1950 MHz for IMT band) and output power to -10 dBm.
7. Ensure DC power supply is disabled and RF output of a signal generator is OFF.
8. Connect evaluation board to the test setup as shown.
9. Turn on DC power supply and measure the idle current.
10. Switch RF output of a signal generator to ON.

11. Increase amplitude of a signal generator to the desired output power level (according to the corresponding data sheet).
12. Measure and record ACP, Gain (as a difference between Input and Output power levels) and total current consumption.

**Test sequence (Recommended PA turn-on and turn-off sequences):**

**Turn-on sequence:**

1. Connect DUT according to the setup shown on Figure 3. **Do not** turn on DC power supply before connecting DUT to RF input and output cables (make sure that RF output of a signal generator is OFF before connecting RF cables to DUT).
2. Turn on  $V_{BATT}$  and  $V_{CC}$  first and then turn on  $V_{EN}$  and  $V_{MODE1}$ .
3. Turn RF output of a signal generator ON and make measurements.

**Turn-off sequence:**

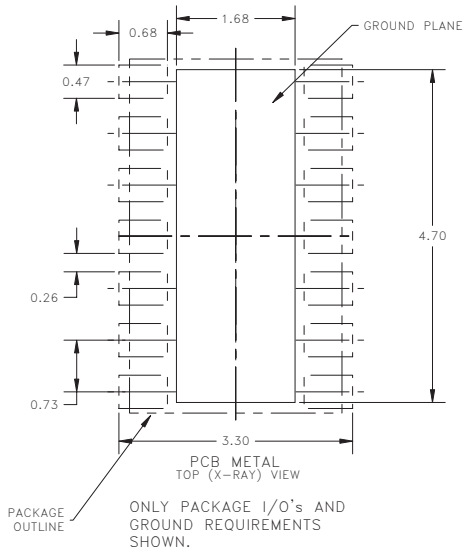
1. Turn RF output of a signal generator OFF. **Do not** disconnect DUT from RF input and output cables before turning off DC power supply.
2. Turn off  $V_{EN}$  and  $V_{MODE1}$ , and then  $V_{BATT}$  and  $V_{CC}$ .
3. Disconnect DUT from the test setup.

**PCB BOARD DESIGN GUIDELINES**

Refer to Figure 4 for the recommended PCB metal design, soldermask design, and stencil print patterns when assembling with ANADIGICS modules.

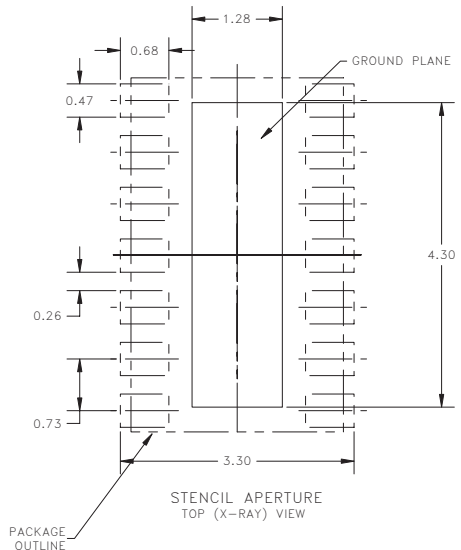
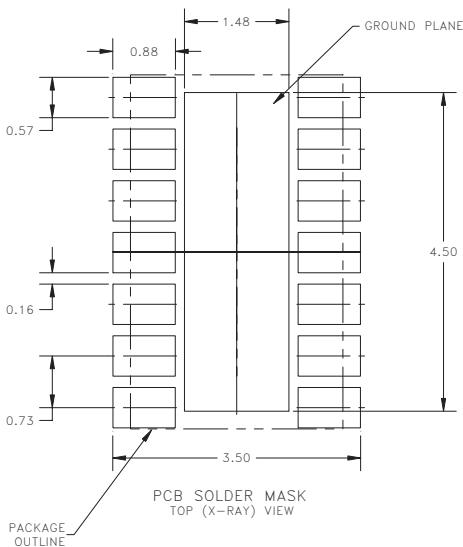
It is important to note that the PCB metal design is dependent upon several factors: the electrical and thermal performance requirements of the product, and the PCB-to-device interconnect pattern. The

PCB metal design recommendations primarily deal with the PCB-to-device interconnection. Specific board-level electrical and thermal performance requirements will be dictated by the physical geometry of the specific application and are the responsibility of the end product manufacturer.



NOTES:

- (1) OUTLINE DRAWING REFERENCE: P8002311
- (2) UNLESS SPECIFIED DIMENSIONS ARE SYMMETRICAL ABOUT CENTER LINES SHOWN.
- (3) DIMENSIONS IN MILLIMETERS.



**Figure 6: PCB Board Design Guidelines**

## Thermal Considerations

In PA module very little heat is dissipated to the air through the top surface of the mold compound. The major thermal path for heat dissipation from the heat sources on the device is the path from the die to the package substrate, to the PCB, and through the PCB surfaces to the air.

The efficiency of heat dissipation (measured by the device junction temperature) is largely dependent on the thermal resistance of the package and the PCB (including the thermal resistance of the PCB to the ambient air):

$$T_j = \Delta T_{ja} + T_a = P (R_{Pkg} + R_{PCB}) + T_a$$

where,

- $T_j$  is the junction temperature of the PA
- $\Delta T_{ja}$  is the temperature difference between the junction and the ambient
- $T_a$  is the ambient temperature
- $P$  is the total power dissipation from the PA
- $R_{Pkg}$  is the thermal resistance of the PA package
- $R_{PCB}$  is the thermal resistance of the PCB and PCB to ambient air.

For a given maximum junction temperature,  $T_{j\max}$ , the maximum power that can be dissipated through the package and the PCB to the ambient air is determined by:

$$P_{\max} = \frac{T_{j,\max} - T_a}{R_{Pkg} + R_{PCB}}$$

This shows that in order to reduce the junction temperature or to dissipate more power from the device, the thermal resistances of the package, the PCB, and the PCB-to-ambient air must be minimized. Thermal resistance of the package is determined by the package size, materials, and structures. High thermal conductivity die attach materials are used. Thermal vias and large metal pads are implemented in the substrate to minimize the thermal resistance and enhance the efficiency of the heat dissipation from the device to the PCB.

When assembled onto a PCB, the package center ground pad for an effective thermal path. Almost all the heat generated from the package must eventually dissipate through the PCB to the air.

Since the PCB-to-air thermal resistance is the major portion of the overall thermal resistance, appropriate design of the system PCB and proper assembly of the package onto the PCB are crucial to overall system thermal performance.

The following guidelines should be considered for PCB designs and board level assembly.

Optimize the board level attachment process and minimize the voids in the solder joints.

Maximize the common ground copper planes in the PCB at the top and the bottom surfaces. More copper content in the inner layers of the PCB can also help reduce the thermal resistance of the PCB.

Ensure sufficient thermal vias connect the top and bottom ground copper planes in the PCB. These are most effective when as many as possible are placed under the PA ground pad. Effectiveness of thermal vias diminishes the farther from the package ground pad they are placed.

Minimize the interaction of the PA package with other heat sources on the PCB. Heat sources near the package can increase the PCB temperature and thus increase the ambient temperature. This is especially critical for the double-sided assembly where placement of heat sources should be avoided in the PCB area opposite the PA site. Conversely, passive components on the PCB can increase the efficiency of heat dissipation from the PCB to the air. Passive components placed near the PA package on either side of the PCB can improve the efficiency of heat dissipation from the PA package.

Increase the contact areas between the PCB and the case, such as the phone case. Heat transfer is much more efficient via conduction than convection. More contact area increases the heat dissipation to the case and eventually to the air.

In general, a larger PCB area is better for heat dissipation through the PCB to the ambient air. A large PCB should be used if allowable by the system design.

Thermal Vias

To improve thermal and electrical performance of a mounted PA module, an array of thermal vias placed on the ground pad should be connected to the internal and bottom common ground copper planes of the PCB. The number of vias is based on via configuration and the thermal and electrical requirements of the particular module under consideration. In general, there is a direct correlation between the thermal via cross-sectional area and the heat dissipation rate. However, the heat dissipation rate through thermal vias can be easily saturated once it is greater than that of solder joint or package heat sink. Large and excessive thermal vias may introduce more voids in the solder joint and actually reduce overall heat dissipation performance.

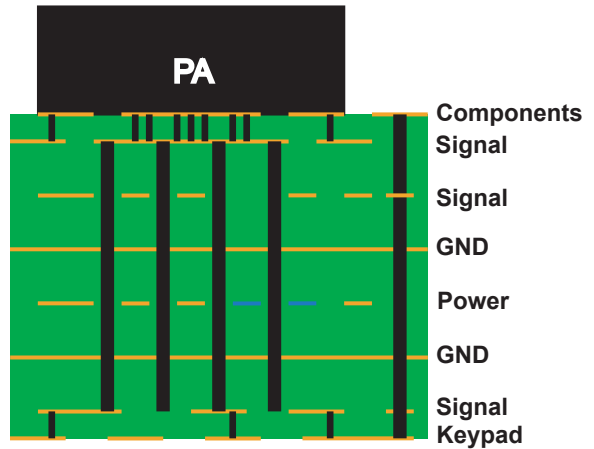
Recommended thermal vias are 0.30 mm to 0.33 mm in diameter, and via barrels should be plated with 1 oz. of copper to plug the vias. The thermal via array should be arranged evenly with a pitch of 0.5 mm to 1.2 mm, depending on the form factor of the package. For the exposed region of the ground pad, if the plating thickness is not sufficient to effectively plug the barrel of the via when plated, solder mask should be used to cap the vias with a minimum dimension equal to the via diameter plus 0.1 mm. This will prevent solder wicking through the thermal via during the soldering process, resulting in voiding.

Another way to plug thermal vias uses solder mask tenting on the bottom of the copper plane. Solder mask tenting must completely cover the vias.

**GROUNDING**

Good grounding is crucial for best performance. “Local ground planes” only connected to the board GND plane using a few microvias is not adequate. All GND planes must be connected to the main GND layer (one designated inner layer of the PCB) using a lot of through vias. Besides being the reference for the all RF and other signals, the GND plane is also used to distribute the heat dissipated by the PA and should therefore be of sufficient size and with many through vias to spread the heat to other copper layers. In order to establish a good ground connection for the PA, it is necessary to assign an area on the

first inner layer to GND. Microvias will go from the large GND pad under the PA to the area on the inner layer and buried or through vias will go the rest of the way to the ground plane in the center of the board. See **Figure 5**.



**Figure 7: Example of PCB Stack-up with Microvias from Top to Bottom Layers, Buried Vias From Layers 2 to 7, and through Vias from Layer**

## Reflow Specifications

The reflow profile is a critical part of the PCB assembly process. A proper reflow profile must provide adequate time for flux volatilization, proper peak temperature, time above liquidous, ramp up and cool down rates. The profile used has a direct bearing on manufacturing yield, solder joint integrity, and the reliability of the assembly [3]. A typical reflow profile is made up of four distinct zones: the preheat zone, the soak zone/flux activation zone, the reflow zone, and the cooling zone [4].

### Preheat Zone

Typically the heating rate in the preheat zone should be 2 °C to 4 °C/second and the peak temperature in this zone should be 100-125 °C. If the temperature ramp is too fast, the solder paste may splatter and cause solder balls. Also, to avoid thermal shock to sensitive components such as ceramic chip resistors, the maximum heating rate should be controlled.

### Soak Zone

The soak zone is intended to allow the board and components to reach a uniform temperature, minimizing thermal gradients. The soak zone also acts to activate the flux within the solder paste. The ramp rate in this zone is very low and the temperature is raised near the melting point of solder (183 °C for standard 63Sn27Pb solder). The consequences of being at too high a temperature in the soak zone are solder balls due to insufficient fluxing (when the ramp rate is too fast) and solder splatter due to excessive oxidation of paste (when the ramp rate is too slow). Typical soak times are usually around the range of 130 –170 °C for 60 to 90 seconds.

### Reflow Zone

In this zone the temperature is kept above the melting point of the solder for 30 to 60 seconds. The peak temperature in this zone should be high enough for adequate flux action and to obtain good wetting. For standard 63Sn37Pb solders, a peak temperature range of 215 – 220 °C is generally considered acceptable

The temperature, however, should not be so high as to cause component damage, board damage, discoloration or charring of the board. Extended duration above the solder melting point will damage temperature sensitive components and potentially create excessive intermetallic growth between the solder and the I/O pad metallization which makes the solder joint brittle and reduces solder joint fa-

tigue resistance. Additionally high temperatures can promote oxide growth, depending upon the furnace atmosphere, which can degrade solder wetting.

### Cooling Zone

The cooling rate of the solder joint after reflow is also important. For a given solder system, the cooling rate is directly associated with the resulting microstructure which in turn, affects the mechanical behavior of solder joints. The faster the cooling rate, the smaller the grain size of the solder will be, and hence the higher the fatigue resistance of the solder joint. Conversely, rapid cooling will result in residual stresses between TCE mismatched components. Therefore the cooling rate needs to be optimized. The profile of choice can affect any of the following areas, to a different degree, by one of more of the profile zones [3].

- Temperature distribution across the assembly
- Plastic IC package cracking
- Solder balling
- Solder beading
- Wetting ability
- Residue cleanability
- Residue appearance and characteristics
- Solder joint voids
- Metallurgical reactions between solder and substrate surface
- Board flatness
- Microstructure of solder joints
- Residual stress level of the assembly

**REFLOW PROFILES**

**Table 3** provides a breakdown of the reflow conditions provided by the JEDEC standard J-STD-020C [5] for leadfree solders. While this standard specifies a peak reflow temperature of 260 °C, the actual peak

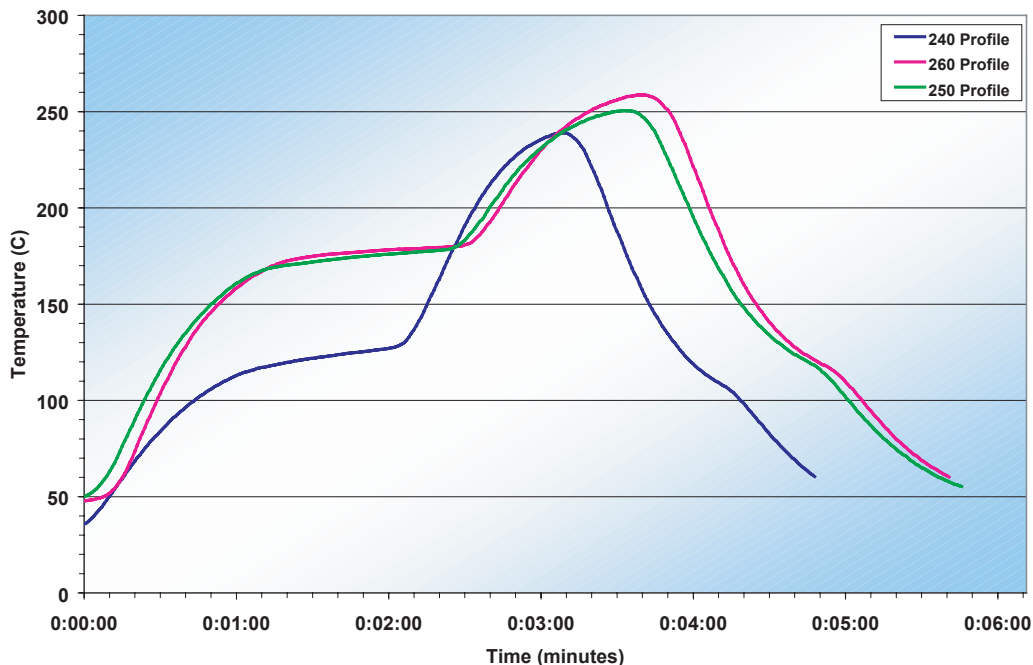
temperature subjected to the parts during qualification will be dependant on the particular products' high temperature tolerating capabilities.

**Table 3: Lead-free MSL Reflow Profile Breakdown**

	<b>JEDEC specifications</b>
Avg. Ramp-up ( $T_L$ to $T_p$ ) <sup>(1),(2)</sup>	3 °C/second max
Dwell Time (175 ± 25 °C)	60-80 seconds
Ramp-up 200 °C to 217 °C	3 °C/second max
Time Above 217 °C	60-150 seconds
Time Within 5 °C of Peak	20-40 seconds max
Peak Temperature <sup>(3)</sup>	260 -5/+0 °C
Average Ramp-down	6 °C/second max

**Notes:**

- (1)  $T_L$  is the solder eutectic temperature.**
- (2)  $T_p$  is the peak temperature.**
- (3) Actual peak temperature will be product independent.**



**Figure 8: Comparison of High Temperature Reflow Profiles**

## REWORK GUIDELINE

The most common method of repairing surface mount devices is by using hot air devices. During this rework process care should be taken to prevent thermal damage to adjacent component or substrates. The following guidelines should be used to prevent thermal damage and to produce an acceptable solder joint after repair/rework [1]:

- Characterize the rework process carefully so as not to overheat and damage the device.
- Keep the number of times a part is removed and replaced to a maximum of two.
- Preheat the substrate for about 30 minutes to about 95 °C.
- Use an appropriate attachment to direct the flow of hot air to the component to be removed or replaced.
- Minimize the heat time to reduce the device exposure to high temperatures.

## REFERENCES

[1] Ray P. Prasad; *Surface Mount Technology - Principles and Practice*; Van Nostrand Reinhold – New York; 1989; Pages 311-328.

[2] <http://www.tutorialsweb.com/smt/smt.htm>

[3] Charles Harper; *Electronic Packaging and Interconnect Handbook*; “Solder Technologies for Electronic Packaging Assembly”; McGraw-Hill 2000; Pages 6.1-6.83.

[4] <http://www.ecd.com/emfg/instruments/tech1.asp>

[5] JEDEC Standard J-STD-020C. *Moisture/Reflow Sensitivity Classification for non-hermetic Solid State Surface Mount Devices*. July 2004.

[6] ANADIGICS Application Note: Solder Reflow Report. Revision 1.

[7] ANADIGICS Application Note: High Temperature Report. Rev. 3

(8) ANADIGICS Application Note: Soldering Guidelines for Module PCB Mounting Rev 12

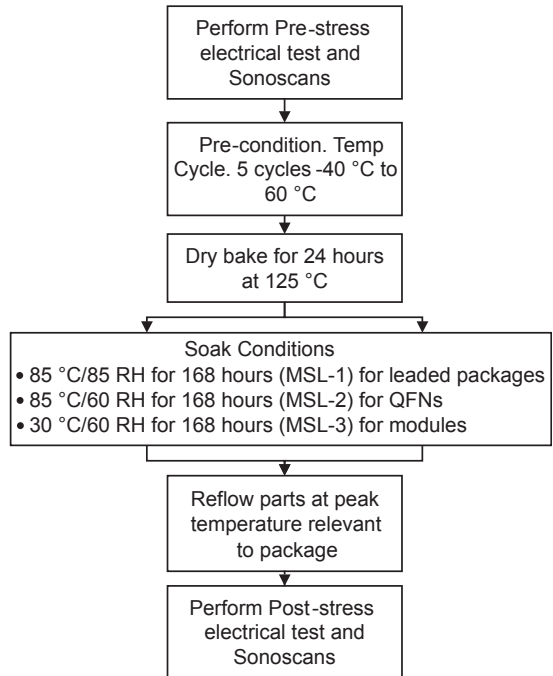
**MSL (Moisture Sensitive Levels)**

MSL levels are used to classify the sensitivity of a microelectronic package to moisture. Packages can be classified from level 1 (hermetic package) to level 6 (very sensitive). Knowledge of the MSL level of a package is crucial during 2nd level solder reflow for proper assembly of the product as these levels dictate the duration that the package can be exposed to the atmosphere before being exposed to solder reflow temperatures. Once this time limit expires, the package is at risk for catastrophic damage during reflow. **Table 4** summarizes the different MSL levels as defined by JEDEC Standards J-STD-020B and J-STD-020C [3, 5].

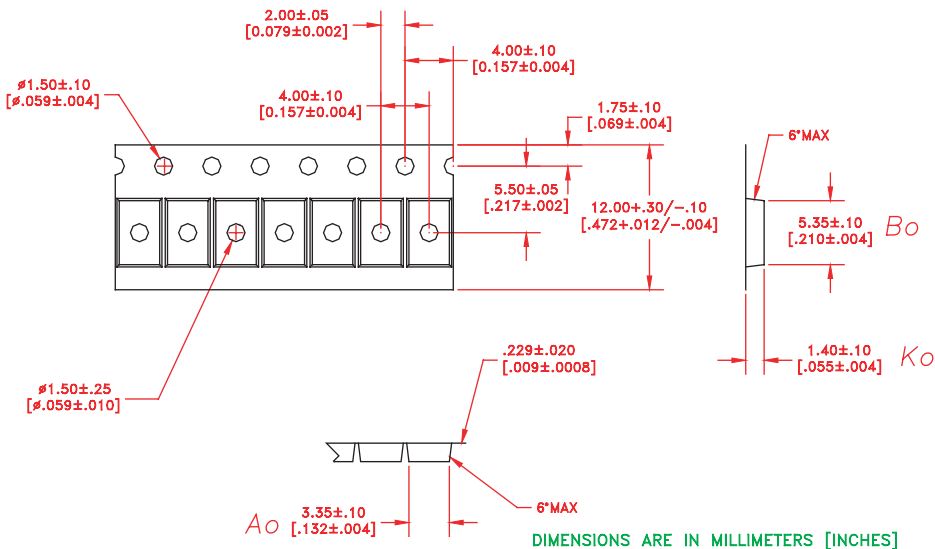
The following flowchart shows the flow of the tests performed to determine the MSL Rating:

**Table 4: Moisture Sensitive Levels Table**

Level	Floor Life
1	Unlimited
2	1 year
2a	4 weeks
3	168 hours (ANADIGICS Product)
4	72 hours
5	48 hours
5a	24 hours
6	Time on Label



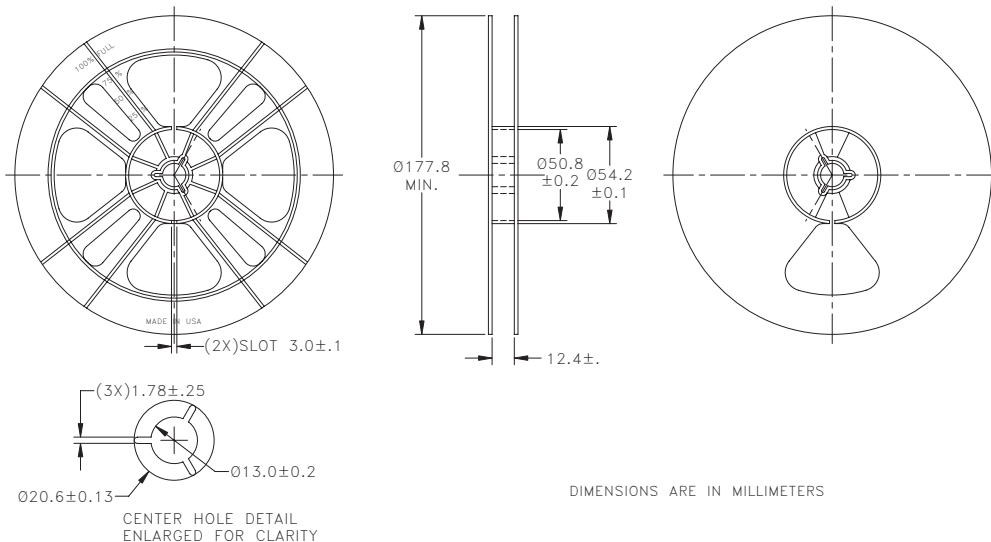
TAPE AND REEL INFORMATION - 3 mm x 5 mm



NOTES:

- 1. MATERIAL: 3000 (CARBON FILLED POLYCARBONATE)  
100% RECYCLABLE.

Figure 9: Carrier Tape drawing



NOTES:

- 1. MATERIAL: BLACK CARBON POLYSTYRENE
- SURFACE RESISTIVITY: 1X10<sup>4</sup> TO 1X10<sup>5</sup> ohms/square

DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

Figure 10: Reel drawing

## ESD (Electro Static Discharge)

ESD or Electro Static Discharge is the leading cause of electronic component failure during and after the manufacturing process. High frequency and highly miniaturized active components are especially prone to damage by ESD. GaAs MMICs are not immune, and deserve every possible ESD precaution.

ESD can damage all electronic parts, components, and subassemblies at all manufacturing and handling stages. It affects production yields, manufacturing costs, product quality, reliability, and profitability. And while only a few components will be catastrophically damaged to an extent where they fail completely, many more may suffer damage that is not immediately apparent. These latent failures will cause premature failure in the field, with huge associated costs.

Thus, ESD impacts productivity and product reliability in all aspects of the electronic environment. In view of all this, the importance of effective ESD prevention cannot be overemphasized.

### GENERAL ESD PRECAUTIONS

General ESD precautions center on measures that can be taken to minimize electrostatic charge build-up. Reducing static generating processes throughout the manufacturing flow should be the goal. Contact and separation of dissimilar materials and common plastics should be avoided as much as possible in the work environment. In addition, general measures to dissipate and neutralize charges should be instituted.

These include:

1. **Humidity Control.** Charge accumulation is minimized if environmental humidity levels are kept high. Forty percent relative humidity is recommended.

For instance, picking up a poly bag from a bench can generate up to 20,000 Volts of charge at less than 25% Relative Humidity, but will generate less than 1,200 Volts if the Relative Humidity is kept between 65% and 90%.

2. **Ionizers.** In situations where we have to deal with isolated conductors that cannot be grounded, and with most common plastics, air ionization can neutralize the static charge. Because only air is required for ionization to be effective, air ionizers can and should

be used wherever it is not possible to ground everything. Ionizers should also be used as a backup where grounding and other methods are also employed.

3. **Wrist straps.** Since the main cause of static is people, the importance of wrist-straps in the fight against ESD cannot be over-emphasized. A wrist-strap, when properly grounded, keeps a person wearing it near ground potential and static charges do not accumulate. Wrist-straps should be worn by all personnel in all ESD Protected Areas, that is, where ESD susceptible devices and end products containing them are assembled, manufactured, handled and packaged.

Further ESD protection, similar to wrist-straps, involves the use of ESD protective floors in conjunction with ESD control footwear or foot-straps. Static control garments (smocks) give additional protection, especially in clean room environments.

4. **Work Areas.** All areas where components that are not in ESD protective packaging are handled should be designated as ESD Protective Areas. Access to such areas should be controlled, and only entered if protective measures, such as wrist-straps and ESD footwear are employed by all personnel. Workstations in such areas should have a static-dissipative work surface with a common ground for it and the worker's wrist-strap.



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