RELEVANT PRODUCTS
- AWT6264
- AWM6268
- AWT6283
- AWB Series PAs

TOPICS COVERED
VREF Biasing
VCC1/VCC2 and VREF RF Sequencing
VREF Switching
VATT biasing and termination
VDET termination
Measuring On/Off Switching Speed

VREF BIASING
ANADIGICS’ lineup of 3G/4G LTE/WiMAX/WCDMA Power Amplifier Modules (PAMs) incorporate a reference voltage, “VREF,” which is an external bias voltage independent of the nominal VCC1/VCC2 supplies. The VREF is used to place the amplifier module into either the “active” or the “idle” state, and to set the operating points of the amplifier’s constituent gain stages. This section reviews the general guidelines that should be followed with respect to biasing the VREF, and discusses the effect of variations in VREF bias magnitude on overall amplifier performance.

The internal bias points for each amplifier part number must be set differently, due to the wide range of operating frequencies and output power levels that are supported by the product portfolio. Please consult the appropriate data sheet for the range of VCC1/VCC2 and VREF voltages that are recommended for a specific device. Data sheets also contain information regarding the nominal reference current “IREF” consumed by each product’s VREF circuit.

Achieving the optimum linearity, gain, and efficiency at the specified level of output power is predicated upon maintaining the proper biasing at both the VCC and the VREF ports. Performance will be compromised if the magnitude of the VREF voltage is allowed to deviate outside of the recommended range. A lower-than-specified VREF voltage will result in abnormally low current consumption which may cause degradation in the device performance, especially over the operating temperature range.

In fact, it is strongly advised that the magnitude of VREF should never be allowed to fall below 2.80Vdc under any circumstances. Conversely, an excessively high VREF will over-stress the amplifiers and reduce their operational lifetimes. Figures 1 thru 4 depict typical variations in EVM, Spectrum Mask (SM), Spectrum Emission Mask (SEM), and Icc/Efficiency that result as the VREF is adjusted over the range from 2.70Vdc to 3.00Vdc at a temperature of +25 °C. Note that the excursions in linearity performance will be greater at reduced or elevated operating temperatures if the VREF is not precisely controlled. In addition, the VREF voltage is the primary determinant that governs the device’s overall current consumption.

VCC1/VCC2 & VREF SEQUENCING
Power-up and power-down sequencing recommendations must be followed to avoid damage to the PA Module. Power-up is initiated by applying the specified DC voltage to VCC1/VCC2 with the VREF bias at 0V. Next, the bias voltage is applied to VREF. RF Drive is applied during the duration of time that the VREF is active.

Power-down is performed in reverse. First, the RF Drive is disabled. Next, the VREF bias voltage is disabled. And, finally, the VCC1/VCC2 voltage is removed. Alternatively, the PA Module may be powered-down by removing the bias from VREF while maintaining the voltage at VCC1/VCC2. Under no circumstances should VREF be applied when no voltage is present at VCC1/VCC2.

VREF SWITCHING
Dynamic switching of the amplifier module between the “active” state and the “idle” state is accomplished by switching the magnitude of the bias voltage applied to the VREF pin. The “active” state voltage is equivalent to the normal operating VREF voltage (2.85Vdc) referenced above. The nominal required “idle” state voltage is 0.0Vdc with a maximum level of 0.5Vdc allowed.

Each ANADIGICS Power Amplifier Module Evaluation Board (EVB) assembly is supplied with a large-value bypass capacitor (0.1uF) that is attached from the VREF
Figure 1: Typical EVM as a function of \( V_{\text{REF}} \) at +25 °C

Figure 2: Typical SPECTRUM MASK as a function of \( V_{\text{REF}} \) at +25 °C
Figure 3: Typical SPECTRUM EMISSION MASK as a function of VREF at +25 °C

Figure 4: Typical ICC/EFFICIENCY as a function of VREF at +25 °C
pin to ground. This amount of bypassing/filtering is desirable when operating the amplifier in a steady-state mode during initial amplifier evaluation and system calibration. However, all reactive elements must be removed from the $V_{\text{REF}}$ pin if dynamic operation is to be implemented, especially if operation in a TDD Wireless System is to be implemented.

It is recommended that a well-regulated voltage be applied to the $V_{\text{REF}}$. A simple resistive divider is not recommended due to the variation in resistance as well as the current through the $V_{\text{REF}}$ pin over extended operating temperature. The current that must be sourced to the $V_{\text{REF}}$ pin varies with each amplifier type and is within a range of 3mA to 15mA.

Most generally available Wireless Transceiver chips incorporate an optional regulated output voltage designated as “AMPLIFIER BIAS”, “PA BIAS”, or equivalent. An internal DAC combines with an LDO to generate the desired magnitudes of voltage and current and is programmable in conjunction with the other transceiver functions. Dynamic switching of the amplifier bias including turn-on and turn-off delay intervals are user-programmable as well.

However, not all Wireless Transceiver chips are capable of sourcing the appropriate amount of current that is necessary to drive the $V_{\text{REF}}$. An alternative option is to incorporate a dedicated voltage regulator in combination with a switching transistor. This approach is illustrated below in Figures 5 - 6 and Table 1 that depict the schematic, bill-of-materials, input/output transfer function, and $V_{\text{REF}}$ voltage over temperature.

The worst-case switching speed of this circuit has been verified to be 100nSec with a current load of 20mA, and the stability of the $V_{\text{REF}}$ voltage is within +/-20mV from -55 °C to +100 °C. Note that the TX$_{\text{EN}}$ must be pulled “low” to enable the amplifier according to the Truth Table contained within the schematic diagram. A “floating” TX$_{\text{EN}}$ forces the amplifier to a disabled condition.

**Circuit Considerations**

The NATIONAL LP2980-ADJ voltage regulator is designed as a low-dropout/low-noise adjustable-output unit. The value of regulator output voltage is determined by the combination of R1 and R2 as defined by the equation published in the data sheet. The R1/R2 voltage divider result is fed back into the regulator (pin 4) and compared to an internal voltage

![Figure 5: External $V_{\text{REF}}$ Switching Circuit Voltage over Temperature](image-url)
General Biasing Considerations for AWB, AWM and AWT Series of Power Amplifier Modules

Figure 6: External High Current V_{REF} Switching Circuit

<table>
<thead>
<tr>
<th>Ref. Desig.</th>
<th>Value</th>
<th>EIA Footprint</th>
<th>Manufacturer</th>
<th>Manufacturer P/N</th>
<th>Description</th>
</tr>
</thead>
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<tr>
<td>C1</td>
<td>1uF</td>
<td>0402</td>
<td>MURATA</td>
<td>GRM155R60J105KE19D</td>
<td>CAP ML CER 1uF 6.3V X5R 0402</td>
</tr>
<tr>
<td>C2</td>
<td>7pF</td>
<td>0201</td>
<td>MURATA</td>
<td>GRM0335C1E7R0DD01D</td>
<td>CAP ML CER 7pF 25V C0G 0201</td>
</tr>
<tr>
<td>C3</td>
<td>4.7uF</td>
<td>1206</td>
<td>VISHAY/SPRAGUE</td>
<td>TR3A475K010C1000</td>
<td>CAP TANT 4.7uF 10V 1206</td>
</tr>
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<td>R1</td>
<td>68.1k</td>
<td>0201</td>
<td>VISHAY/DALE</td>
<td>CRCW020168K1FKED</td>
<td>RES THK FLM 1% 68.1K 0201 1/20W</td>
</tr>
<tr>
<td>R2</td>
<td>49.9k</td>
<td>0201</td>
<td>VISHAY/DALE</td>
<td>CRCW020149K9FKED</td>
<td>RES THK FLM 1% 49.9K 0201 1/20W</td>
</tr>
<tr>
<td>R3</td>
<td>360k</td>
<td>0201</td>
<td>ROHM</td>
<td>MCR006YZPJ364</td>
<td>RES THK FLM 5% 360K 0201 1/20W</td>
</tr>
<tr>
<td>R4</td>
<td>560</td>
<td>0201</td>
<td>ROHM</td>
<td>MCR006YZPJ561</td>
<td>RES THK FLM 5% 560 0201 1/20W</td>
</tr>
<tr>
<td>Q1</td>
<td>NTK3139P</td>
<td>SOT-723</td>
<td>ON SEMICONDUCTOR</td>
<td>NTK3139P</td>
<td>MOSFET, P-CHANNEL</td>
</tr>
<tr>
<td>U1</td>
<td>LP2980-ADJ</td>
<td>SOT-23 (5L)</td>
<td>NATIONAL</td>
<td>LP2980IM5-ADJ/NOPB</td>
<td>V REG, LDO, 50mA, ADJUSTABLE</td>
</tr>
</tbody>
</table>

Table 1: External High Current V_{REF} Switching Circuit Bill-of-Materials
General Biasing Considerations for AWB, AWM and AWT Series of Power Amplifier Modules

reference. It is recommended that high-precision 1% tolerance resistors be used for R1 and R2 to facilitate proper adjustment of the output voltage.

The **ON NTK3139P** MOSFET is selected as the best available compromise of package size, power dissipation capability, turn-on threshold, and switching speed. Note that a small but discernable voltage drop will be present across the MOSFET. Therefore, the final values of R1 and R2 should be determined from the voltage as measured at pin 3 (drain) of the MOSFET and not pin 5 of the voltage regulator.

Capacitive elements (C1, C2, C3) are as-recommended in the voltage regulator data sheet. They should be located as close to the voltage regulator as possible. Special attention must be given to the composition of capacitor C3. A high-quality solid tantalum capacitor must be used because its characteristic ESR (effective series resistance) is approximately 1Ω. This resistance is recommended to maintain voltage regulator stability. A ceramic capacitor characterized by an ultra-low series resistance (50mΩ) may be substituted for a solid tantalum capacitor only if a 1Ω series resistor is installed as well.

Resistor R3 (360kΩ) serves as a “pull-up” element to maintain a nominal gate-to-source voltage in the event that the TX

**BIASING and TERMINATION**

Some PA modules incorporate a 20dB attenuator that can be enabled via the VATT pin. The attenuator is activated when a logic level “high” is applied to VATT. The VATT must be pulled to a logic level “low” to disable the attenuator during normal operation. The VATT must be biased either “high” or “low” at all times and must not be allowed to “float” because stray noise, transients, or a random lock-up condition may induce unintended attenuator activation. It is recommended that the VATT pin be grounded through a 100kΩ resistor if the Attenuator pin is not being utilized.

**VDET TERMINATION**

Various PA modules feature an internal “detector” circuit that generates a DC voltage whose magnitude is proportional to the RF Output signal level. This section of the application note reviews the general guidelines that should be followed to enable proper detector functionality.

**Theory of Operation**

The internal detector circuit samples and rectifies a small portion of the RF Output waveform. The resultant pseudo-DC voltage is available via a pin designated as “VDET”. The voltage is conditioned by an externally-applied circuit as described below.

**External Termination Circuit**

A simple passive RC “termination network” is connected to the VDET pin, as shown in Figure 7, to filter ripple and other perturbations that may be present in the output voltage. The resulting curve of VDET voltage as a function of the RF output power is graphed in Figure 8.

The elemental values yield a large RC Time Constant that is suited to eliminating low-frequency noise. This characteristic is desirable when operating the amplifier in a steady-state mode during initial amplifier evaluation and system calibration.

However, it may be necessary to evaluate the VDET output when the amplifier is being operated dynamically in a “burst-mode” in a TDD system. In this condition the RF Output (via the Vref or VENABLE pin) is actively switched very rapidly between the “on” and the “off” states at a rate that may exceed the response-time of the VDET termination circuit. Dynamic testing can be accomplished by modifying the component values to yield a lower RC time-constant for a faster response time. The recommended circuit diagram shown in Figure 9 satisfies this requirement.
**General Biasing Considerations for AWB, AWM and AWT Series of Power Amplifier Modules**

**Figure 7: Standard \( V_{\text{DET}} \) Circuit (as Published in Datasheets)**

**Figure 8: Typical \( V_{\text{DET}} \) Voltage Versus RF Output Power**

**Switching Times**

Equations 1.0 and 1.1 define the percentage (%) of the final voltage value that is present in an RC network as a function of the quantity of time-constants that have elapsed. Equation 1.0 is associated with a “charging” condition and equation 1.1 represents the “discharging” condition.

Equation 1.0: Charging \( \% = 100(1 - e^{-t/RC}) \)

Equation 1.1: Discharging \( \% = 100e^{-t/RC} \)

Where \( R \) is the resistance in \( \Omega \), \( C \) is the capacitance in Farads, and \( \tau \) is the quantity of Time-constants.

When Equations 1.0 and 1.1 are graphed, as in Figures 10 and 11, it can be seen that the time required to either charge or discharge the voltage of an RC network to within 1\% of its terminal value is approximately 4 time-constants \( (4\tau) \). The total expected charge or discharge times for each of the two external circuits are listed in the lower-left hand corner of Figures 7 and 9. The recommended resistor and capacitor values are a compromise between minimal response-time and adequate DC filtering.
Figure 9: $V_{DET}$ Circuit Modified for Faster Response Time

Figure 10: $\% = 100(1 - e^{-t/RC})$
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Floating $V_{DET}$ pin:
The $V_{DET}$ output pin must be terminated at all times and not be allowed to “float”. Failure to terminate this pin may induce unpredictable and undesirable behavior. For example, the magnitude of the resultant $V_{DET}$ voltage may not be reliable and consistent, especially over the permissible ranges of ambient operating temperature and output load impedance, and at elevated levels of output power. It is possible for the polarity of the $V_{DET}$ voltage to reverse itself and become “negative” at elevated levels of output power, if the $V_{DET}$ output pin is not properly terminated.

In addition, externally coupled stray noise impulses may propagate into the amplifier stages from the $V_{DET}$ pin and modulate the RF output waveform thereby causing degradation in the linearity performance. As the internal $V_{DET}$ circuit has a limited amount of forward and reverse isolation, it is recommended that a single resistive termination (100kΩ) be implemented as shown in Figure 12 if the $V_{DET}$ function is not required.

$V_{REF}$ Voltage Effects on $V_{DET}$:
The internal $V_{DET}$ circuit derives its DC biasing from the $V_{REF}$ supply voltage. Therefore, the recommended value of $V_{REF}$ voltage, as published in the data sheet, should be maintained to within +/-1.8% whenever possible. Excessive deviations in the $V_{REF}$ voltage may decrease the accuracy of the $V_{DET}$ voltage, as well as degrade the nominal linearity performance of the RF amplifier.

Amplifier Response Time:
Although the RF Output waveform is sampled by the detector circuit during normal operation, the $V_{DET}$ output should not be utilized as a direct monitoring point or as a test point for characterization of the slew-rate of the RF Output waveform when the amplifier is cycled between the “on” and the “off” states. Internal propagation delays artificially lengthen the observed settling time of the RF output waveform. It is recommended that a signal analyzer of sufficient bandwidth be used to directly evaluate the performance of the RF amplifier section in the time-domain.

Closed-loop Power Control:
The overall accuracy of the $V_{DET}$ output voltage may be influenced by non-optimal values of load impedance presented to the amplifier RF Output port. The $V_{DET}$ circuit is passive in nature and hence the overall directivity is limited. It responds equally well to both forward and reflected power. Hence, it is not recommended that the $V_{DET}$ voltage be used as the primary driver in a closed-loop feedback power control circuit.

**Figure 11:** $% = 100e^{-t/RC}$

![Graph](graph.png)

**Formula:** $% = 100e^{-t/RC}$
MEASURING ON/OFF SWITCHING SPEED

The Switching Speed is defined as the time that elapses between the initial application of control voltage into the $V_{REF}$ and the instance at which the detected RF envelope completes the transition from 10% to 90% of its final value as shown in Figure 13. It is recommended, for best accuracy, to use an external high-speed, wide-bandwidth detector such as the ANALOG DEVICES AD8318 for this measurement as outlined in the Block Diagram in Figure 14A. The internal $V_{DET}$ circuit can be used as shown in Figure 14B if an external detector is unavailable; however, the $V_{DET}$ lacks the necessary bandwidth to generate an accurate response-time profile. Therefore, it is recommended that the $V_{DET}$ pin not be used for Switching Speed measurements.

The Switching Speed characterization of an AWB7227 is illustrated in Figures 15 and 16 as an example of the typical detected on/off waveforms that can be
expected with the ANADIGICS PA Modules. The upper trace represents the detected waveform. The waveform polarity in Figures 15A and 16A are inverted due the design of the AD8318. The lower trace represents the driving square wave. Note the differences in response times between the internal $V_{DET}$ and the external detector. The external switching circuit previously presented in Figure 6 may be used as a buffer between the Waveform Generator and the $V_{REF}$ if it is determined that the generator lacks sufficient current-sourcing capability to drive the load presented by the $V_{REF}$ circuit.

The values of the external components terminating the $V_{DET}$ and the $V_{REF}$ pins must be verified as outlined in previous sections prior to commencing the Switching Speed measurement. Specifically, the external $V_{DET}$ circuit must be modified for dynamic operation. In addition, all bypass capacitors must be removed from the $V_{REF}$.

Figure 14A: Switching Speed Test Setup using External Detector (Recommended)

Figure 14B: Switching Speed Test Setup using Internal $V_{DET}$ (Not Recommended)
Figure 15A: “Off-to-On” Switching Speed using External Detector (Recommended)

Figure 15B: “Off-to-On” Switching Speed using Internal $V_{DET}$ (Not Recommended)
Figure 16A: “On-to-Off” Switching Speed using External Detector (Recommended)

Figure 16B: “On-to-Off” Switching Speed using Internal $V_{DET}$ (Not Recommended)
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